



MX28F002T/B

2M-BIT [256K x 8] CMOS FLASH MEMORY

FEATURES

- 262,144 bytes by 8-bit organization
- Fast access time: 70/90/120ns
- Low power consumption
 - 50mA maximum active current
 - 100uA maximum standby current
- Programming and erasing voltage 12V \pm 5%
- Command register architecture
 - Byte Programming (15us typical)
 - Sector Erase (Any one from 5 blocks:16K-Byte x1, 8K-Byte x2, 96K-Byte x1, and 128K-Byte x1)
 - Auto Erase with Erase Suspend capability
- Status Register feature for Device status detection
- Absolute Hardware-Protection for Boot Sector
- Auto Erase (sector) and Auto Program
 - Status Registers
- 10,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1 to VCC+1V
- Package type:
 - 40-pin TSOP(10mm x 20mm)

GENERAL DESCRIPTION

The MX28F002T/B is a 2-mega bit Flash memory organized as 256K bytes of 8 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX28F002T/B is packaged in 40-pin TSOP. It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

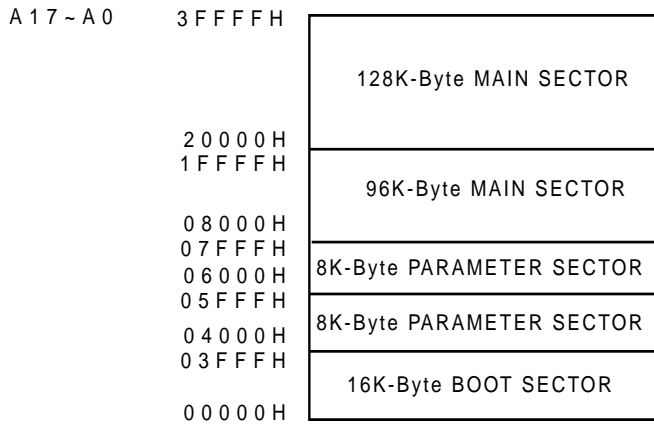
The standard MX28F002T/B offers access times as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX28F002T/B has separate chip enable (\overline{CE}) and output enable (\overline{OE}) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX28F002T/B uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

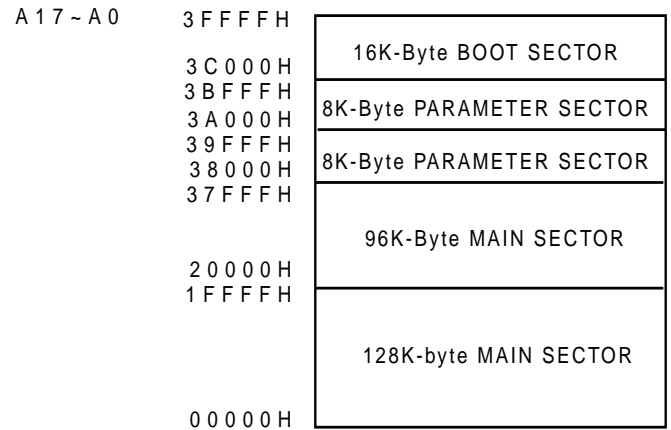
MXIC Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX28F002T/B uses a 12.0V \pm 5% VPP supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

BLOCK STRUCTURE



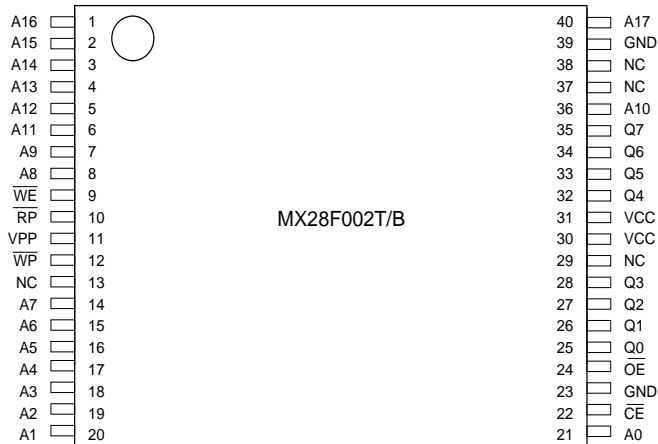
MX28F002-B



MX28F002-T

PIN CONFIGURATIONS

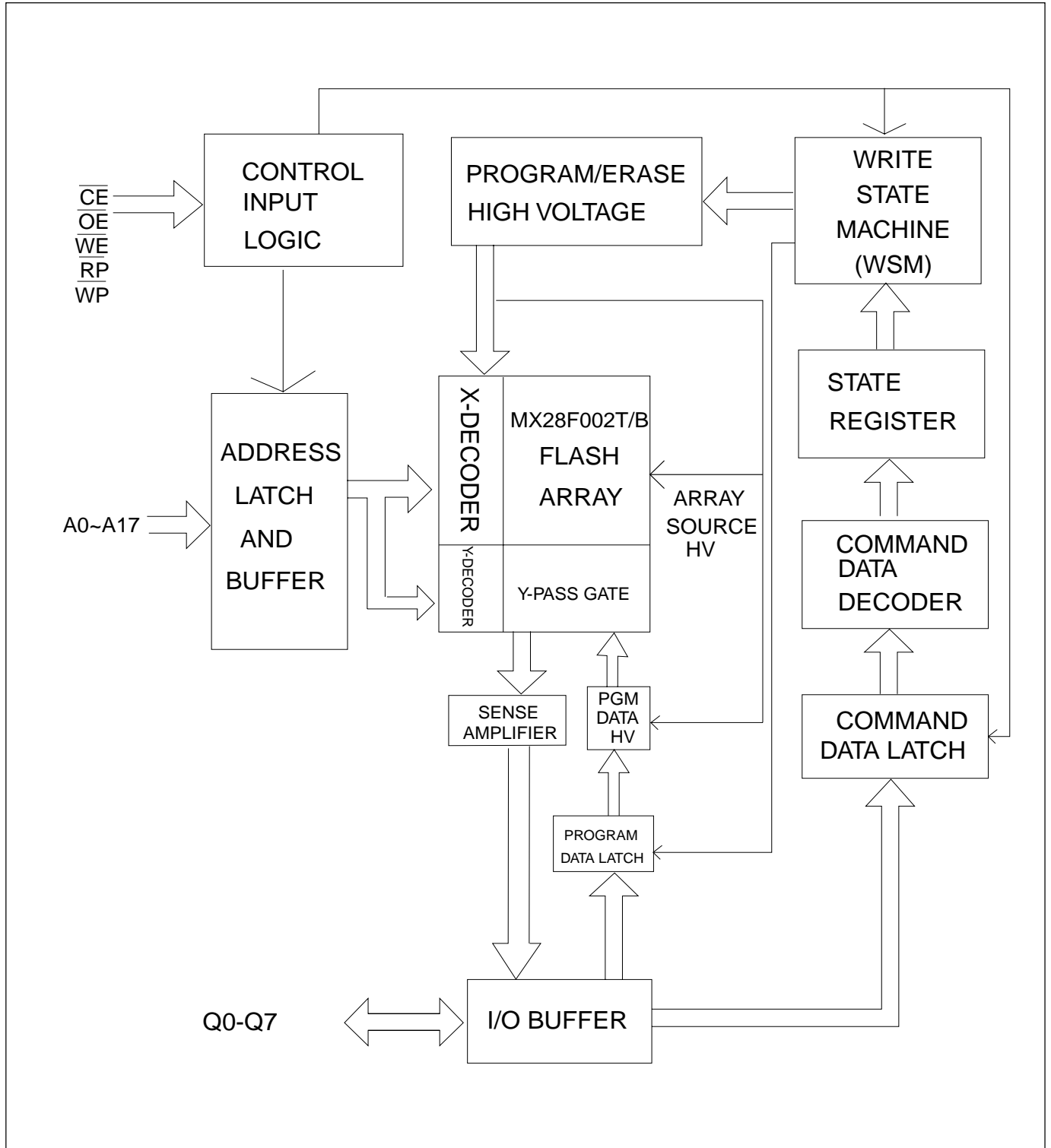
40-TSOP (10mm x 20mm)



PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q7	Data Input/Output
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{RP}	Reset Input
\overline{WP}	Write Protect
\overline{OE}	Output Enable Input
VPP	Power supply for Program and Erase
VCC	Power Supply Pin (+5V)
GND	Ground Pin

BLOCK DIAGRAM



AUTOMATIC PROGRAMMING

The MX28F002T/B is programmable using the Automatic Programming algorithm. The Automatic Programming algorithm does not require the system to time out or verify the data programmed. The typical room temperature chip programming time of the MX28F002T/B is less than 5 seconds.

AUTOMATIC BLOCK ERASE

The MX28F002T/B is block(s) erasable using MXIC's Auto Block Erase algorithm. Block erase modes allow one of 5 blocks of the array to be erased in one erase cycle. The Automatic Block Erase algorithm automatically programs the specified block(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm requires the user to only write a program set-up command and a program command (program data and address). The device automatically times the programming pulse width, provides the program verify, and counts the number of sequences. A status register scheme provides feedback to the user as to the status of the programming operation.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to only write an Erase Set-up command and an Erase command. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verify, and counts the number of sequences. A status register provides feedback to the user as to the status of the erase operation. It is noted that after an Erase Set-up command, if the next command is not an Erase command, then the state-machine will set both the program status and Erase Status bits of the Status Register to a "1", place the device into the read Status Register state, and wait for another command.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses and data is latched on the rising edge of WE.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX28F002T/B electrically erases all within a sector or chip bits simultaneously using Fowler-Nordheim tunneling. The array is programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will respond to Erase Suspend command. After Erase Suspend completed, the device stays at status register Read state. After the state machine has completed its task, it will allow the command register to respond to its full command set.

TABLE 1. SOFTWARE COMMAND DEFINITIONS

COMMAND	BUS CYCLE	FIRST BUS CYCLE			SECOND BUS CYCLE		
		Mode	Address	Data X8	Mode	Address	Data X8
Read Memory Array	1	Write	X	FFH	---	---	---
Setup Auto program/ Auto Program	2	Write	X	10H or 40H	Write	Program Address	Program Data
Setup Erase/Erase(Block)	2	Write	X	60H	Write	Block Address	60H
Setup Auto Erase/ Auto Erase(Block)	2	Write	X	20H	Write	Block Address	D0H
Erase Verify	2	Write	Verify Address	A0H	Read	X	Verify Data
Read device identifier code	2	Write	X	90H	Read	ADI	DDI
Erase Suspend	1	Write	X	B0H	---	---	---
Erase Resume	1	Write	X	D0H	---	---	---
Read Status Register	2	Write	X	70H	Read	X	SRD
Clear Status Register	1	Write	X	50H	---	---	---

Note:

1. Write and Read mode are defined in mode selection table.
2. ADI = Address of Device identifier; A0 = 0 for manufacture code, A0 = 1 for device code.
DDI = Data of Device identifier : C2H for manufacture code, 2DH for device code of MX28F002T; 2EH for device code of MX28F002B
X = X can be VIL or VIH
SRD = Status Register Data

COMMAND DEFINITIONS

Placing high voltage on the VPP pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 1 defines these MX28F002T/B register commands. Table 2 defines the bus operations of MX28F002T/B.

TABLE 2. MX28F002T/B BUS OPERATION

Pins		A0	A9	\overline{CE}	\overline{OE}	\overline{WE}	VPP	Data I/O D0~D7
Mode								
Read-Only	Read	A0	A9	VIL	VIL	VIH	VPPL	Data Out
	Output Disable	X	X	VIL	VIH	VIH	VPPL	Hi-Z
	Standby	X	X	VIH	X	X	VPPL	Hi-Z
	Read Silicon ID(Mfr)(2)	VIL	VID(3)	VIL	VIL	VIH	VPPL	Data=C2H
	Read Silicon ID(Device)(2)	VIH	VID(3)	VIL	VIL	VIH	VPPL	Data=DDI
Read/Write	Read	A0	A9	VIL	VIL	VIH	VPPH	Data Out(4)
	Output Disable	X	X	VIL	VIH	VIH	VPPH	Hi-Z
	Standby(5)	X	X	VIH	X	X	VPPH	Hi-Z
	Write	A0	A9	VIL	VIH	VIL	VPPH	Data In(6)

NOTES:

- VPPL may be grounded, a no-connect with a resistor tied to ground, or $\leq VCC + 2.0V$. VPPH is the programming voltage specified for the device. When VPP = VPPL, memory contents can be read but not written or erased.
- Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1. All other addresses are low.
- VID is the Silicon-ID-Read high voltage, 11.5V to 13V.
- Read operations with VPP = VPPH may access array data or Silicon ID codes.
- With VPP at high voltage, the standby current equals ICC + IPP (standby).
- Refer to Table 1 for valid Data-In during a write operation.
- X can be VIL or VIH.

TABLE 3. SILICON ID CODE

Pins		A0	D7	D6	D5	D4	D3	D2	D1	D0	Code(Hex)
Code											
Manufacture code		VIL	1	1	0	0	0	0	1	0	C2H
Device code for MX28F002T		VIH	0	0	1	0	1	1	0	1	2DH
Device code for MX28F002B		VIH	0	0	1	0	1	1	1	0	2EH

READ COMMAND

While VPP is high, for erasure and programming, memory contents can also be accessed via the Read command. The read operation is initiated by writing FFH into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

RESET COMMAND

A Reset command is provided as a means to safely abort the erase- or program-command sequences. Following Set-up command with two consecutive writes of FFH for ERS(or one write of FFH for PGM) will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

SILICON-ID-READ COMMAND

Flash-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a desired system-design practice.

The MX28F002T/B contains a Silicon-ID-Read operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle with A0=VIL retrieves the manufacturer code of C2H. A read cycle with A0=VIH returns the device code of 2DH for MX28F002T and 2EH for MX28F002B.

ERASE-VERIFY COMMAND

After each erase operation, all bytes must be verified. The Erase Verify operation is initiated by writing A0H into the command register. The address for the byte to be verified must be supplied as it is latched on the rising edge of the \overline{WE} pulse.

The MX28F002T/B applies an internally generated margin voltage to the addressed byte. Reading FFH

from the addressed byte indicates that all bits in the byte are erased.

The Erase-Verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation needs to be performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g. Program Set-up) to the command register. The High Reliability Erase algorithm illustrates how commands and bus operations are combined to perform electrical erasure of the MX28F002T/B.

SET-UP AUTOMATIC BLOCK ERASE/ERASE COMMANDS

The Automatic Block Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Block Erase command and Automatic Block Erase command. Upon executing the Automatic Block Erase command, the device automatically will program and verify the block(s) memory for an all-zero data pattern. The system is not required to provide any controls or timing during these operations.

When the block(s) is automatically verified to contain an all-zero pattern, a self-timed block erase and verify begin. The system is not required to provide any control or timing during these operations.

When using the Automatic Block Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard Erase Verify command is used.

The Automatic Set-up Block Erase command is a command only operation that stages the device for automatic electrical erasure of selected blocks in the array. Automatic Set-up Block Erase is performed by

writing 20H to the command register. To enter Automatic Block Erase, the user must write the command D0H to the command register. Block addresses selected are loaded into internal register on the second rising edge of \overline{WE} . Each successive block load cycles started by the falling edge of \overline{WE} must begin within 30us from the rising edge of the preceding \overline{WE} . And the status register may only be read after all block addresses has been loaded internally (100us after the last address is loaded). Reading prior to this time will disturb the internal block address loading process.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Block Erase operation, and therefore will only be responded to during Automatic Block Erase operation. It is noted that Erase Suspend is meaningful for block erase only after block addresses load are finished (100 us after the last address is loaded). After this command has been executed, the command register will initiate erase suspend mode. The state machine will set DQ7, DQ6 as 1, 1, after suspend is ready. At this time, state machine only allow the command register to respond to the Read Memory Array, Erase Resume and Read Status Register.

ERASE RESUME

This command will cause the command register to clear the suspend state and set DQ6, DQ7, back to 0, 0, but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions.

SET-UP AUTOMATIC PROGRAM/PROGRAM COMMANDS

The Automatic Set-up Program is a command only operation that stages the device for automatic programming. Automatic Set-up Program is performed by writing 10H/40H to the command register. Program command is the command for byte-program.

Once the Automatic Set-up Program operation is performed, the next \overline{WE} pulse causes a transition to an active programming operation. Address Data are internally latched on the rising edge of the \overline{WE} pulse. The rising edge of \overline{WE} also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically

provide an adequate internally generated program pulse and verify margin.

If the program operation was unsuccessful, bit 4 of the Status Register will be set to a "1", indicating a Program failure. If V_{pp} was not within acceptable limits after the program command is issued, the state machine will not execute a program sequence; instead, bit 4 of the Status Register is set to a "1" to indicate a Program Failure, and bit 3 is set to a "1" to identify that V_{pp} supply voltage was not within acceptable limits.

STATUS REGISTER

The device contains a Status Register which may be read to determine when a Program or Erase operation is complete, and whether that operation completed successfully. The Status Register may be read at any time by writing the Read Status command to the command interface. After writing this command, all subsequent Read operations output data from the Status Register until another command is written to the command interface. A Read Array command must be written to the command interface to return to the read array mode. The Status Register bits are output on DQ[0:7].

The contents of the Status Register are latched on the falling edge of \overline{OE} or \overline{CE} , whichever occurs last in the read cycle. This prevents possible bus errors which might occur if the contents of the Status Register change while reading the Status Register. \overline{CE} or \overline{OE} must be toggled with each subsequent status read, or the completion of a Program or Erase operation will not be evident from the Status Register.

When the state machine is active, this register will indicate the status of the state machine, and will also hold the bits indicating whether or not the state machine was successful in performing the desired operation.

CLEARING THE STATUS REGISTER

The state machine sets status bits "3" through "7" to "1", and clears bits "6" and "7" to "0", but cannot clear status bits "3" through "5" to "0". Bits 3 through 5 can only be cleared by the controlling CPU through the use of the Clear Status Register command. These bits can

indicate various error conditions. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several bytes or erasing multiple blocks in sequence). The Status Register may then be read to determine if an error occurred during that programming or erasure series. This adds flexibility to the way the device may be programmed or erased. Once an error occurred, the command

Interface Only responds to clear Status Register, Read Status Register and Read Array. To clear the Status Register, the Clear Status Register command is written to the command interface. Then, any other command may be issued to the command interface. Note, again, that before read cycle can be initiated, a Read Array command must be written to the command interface to specify whether the read data is to come from the Memory Array, Status Register, or Silicon-ID.

Status Register Bit Definition

WSMS	ESS	ES	PS	VPPS
7	6	5	4	3

SR.7 = WRITE STATE MACHINE STATUS(WSMS)
1 = Ready
0 = Busy

SR.6 = ERASE-SUSPEND STATUS (ESS)
1 = Erase Suspended
0 = Erase in Progress/Completed

SR.5 = ERASE STATUS
1 = Error in Erase
0 = Successful Erasure

SR.4 = PROGRAM STATUS
1 = Error in Byte Program
0 = Successful Byte Program

SR.3 = Vpp STATUS
1 = Vpp Low Detect, Operation Abort
0 = Vpp OK

NOTE :

State machine bit must first be checked to determine Byte program or Block Erase completion, before the Program or Erase Status bits are checked for success.

When Erase Suspend is issued, state machine halts execution and sets both WSMS and ESS bits to "1," ESS bit remains set to "1" until an Erase Resume command is issued.

When this bit set to "1," state machine has applied the maximum number of erase pulses to the device and is still unable to successfully verify erasure.

When this bit is set to "1," state machine has attempted but failed to program a byte or word.

The Vpp status bit, unlike an A/D converter, does not provide continuous indication of Vpp level. The state machine interrogates Vpp level only after the Byte Write or Erase command sequences have been entered, and informs the system if Vpp has not been switched on.

DATA PROTECTION

The MX28F002T/B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

LOW VPP WRITE INHIBIT

To avoid initiation of a write cycle during VPP power-up and power-down a write cycle is locked out for VPP less than V_{PPLK} (typically 9V). If $V_{PP} < V_{PPLK}$, the command register is disabled and all internal program/erase circuits are disabled. Subsequent writes will be ignored until the VPP level is greater than V_{PPLK} . It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional write when VPP is above V_{PPLK} .

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns (typical) on \overline{CE} or \overline{WE} will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle \overline{CE} and \overline{WE} must be a logical zero while OE is a logical one.

POWER SUPPLY DECOUPLING

In order to reduced power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND, and between its VPP and GND.

VPP TRACE ON PRINTED CIRCUIT BOARD

Programming flash memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the Vpp power supply trace. The Vpp pin supplies the memory cell current for programming. Use similar trace widths and layout considerations given to the Vcc power bus. Adequate Vpp supply traces and decoupling will decrease Vpp voltage spikes and overshoots.

RESET MODE

This mode is enabled by \overline{RP} pin. During Read modes, \overline{RP} going low deselects the memory and place the output drivers in a high-Z state.

In erase or program modes, \overline{RP} low will abort erase or program operations, but the memory contents are no longer valid as the data has been corrupted by \overline{RP} function. \overline{RP} transition to VIL, or turning power off to the device will clear up Status Register and automatically defaults to the read array mode.

When \overline{RP} is at VHH, the boot block is unlocked and can be programmed or erased.

WRITE PROTECT

Provides a method for unlocking the boot sector in a system without a 12V supply. WP must be pulled to logic low or high, not left floating.

When \overline{WP} is at logic low, the bootsector is locked, preventing Program and Erase operations to the boot sector.

When \overline{WP} is at logic high, the bootsector is unlocked and can be programmed or erased.

This feature is overridden and the boot sector unlocked when RP is at VHH.

POWER-UP SEQUENCE

The MX28F002T/B powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two-step command sequence. Vpp and Vcc power up sequence is not required.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
A9 & VPP & \overline{RP}	-0.5V to 13.5V

NOTICE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:

Specifications contained within the following tables are subject to change.

SWITCHING VCC VOLTAGES

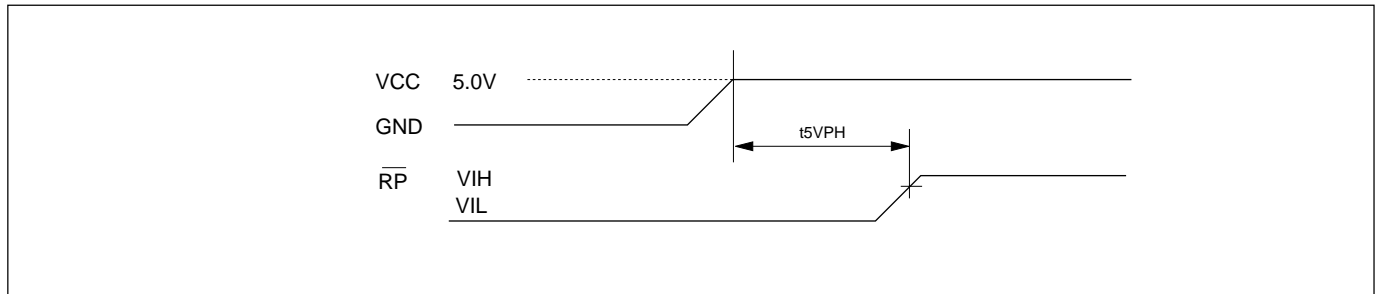
VCC SUPPLY SWITCHING TIMING

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T5VPH	VCC at 4.5V (minimum) to \overline{RP} High	3		ms

NOTICE:

The T5VPH time must be strictly followed to guarantee all other read and write specifications.

VCC SUPPLY SWITCHING WAVEFORM



CAPACITANCE TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			8	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOU = 0V

READ OPERATION
DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10%, VPP = GND to VCC

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			1	uA	VIN = GND to VCC
ILO	Output Leakage Current			10	uA	VOUT = GND to VCC
IPP1	VPP Current		1	100	uA	VPP = 5.5V
ISB1	Standby VCC current			2	mA	$\overline{CE} = V_{IH}$
ISB2			1	100	uA	$\overline{CE} = V_{CC} + 0.3V$
ICC1	Operating VCC current			50	mA	IOUT = 0mA, f=1MHz
ICC2				70	mA	IOUT = 0mA, f=10MHz
VIL	Input Low Voltage	-0.3(NOTE 1)		0.8	V	
VIH	Input High Voltage	2.0		VCC + 0.3	V	
VOL	Output Low Voltage			0.45	V	IOL = 2.1mA
VOH	Output High Voltage	2.4			V	IOH = -400uA

NOTES:

- VIL min. = -1.0V for pulse width ≤ 50 ns.
VIL min. = -2.0V for pulse width ≤ 20 ns.
- VIH max. = VCC + 1.5V for pulse width ≤ 20 ns
If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%, VPP = GND to VCC

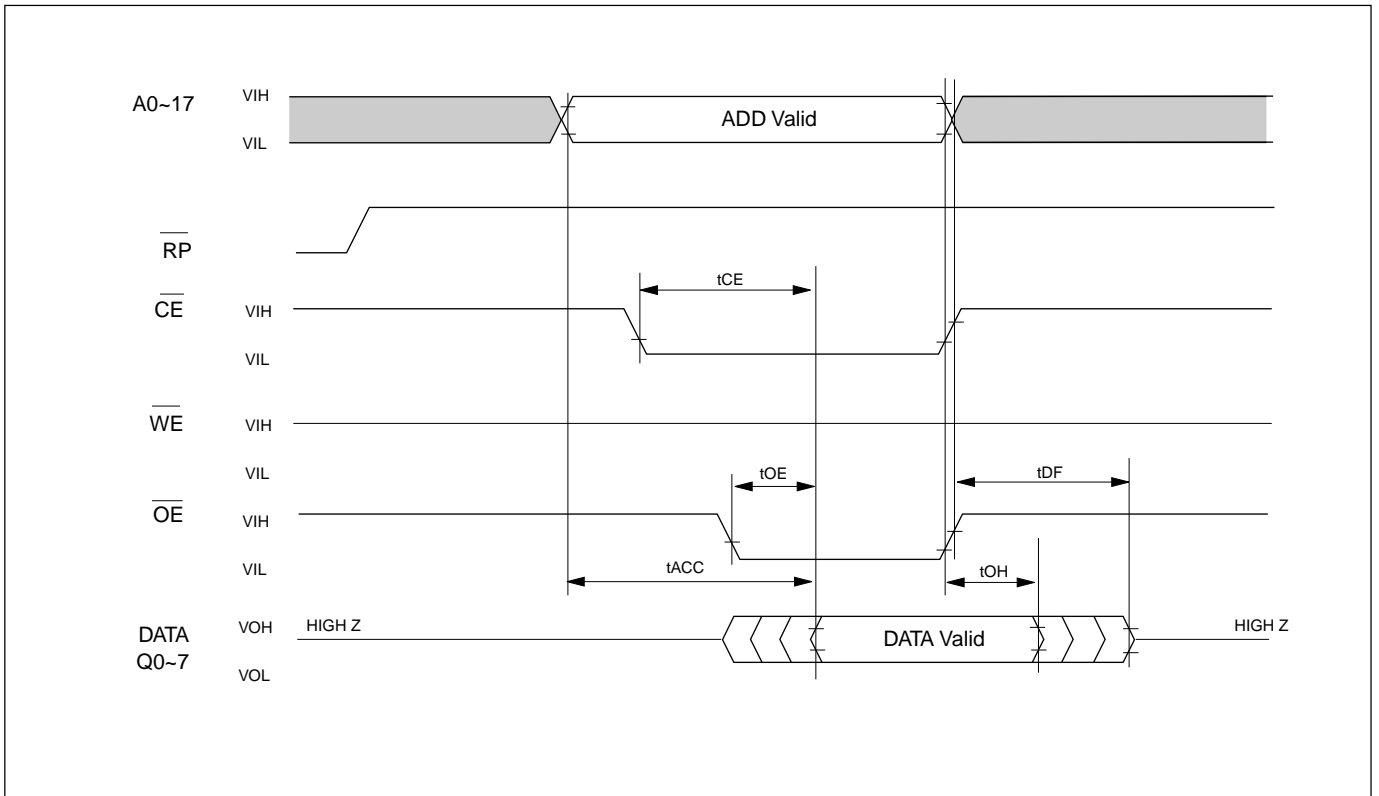
SYMBOL	PARAMETER	28F002T/B-70		28F002T/B-90		28F002T/B-12		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
tACC	Address to Output Delay		70		90		120	ns	$\overline{CE}=\overline{OE}=V_{IL}$
tCE	\overline{CE} to Output Delay		70		90		120	ns	$\overline{OE}=V_{IL}$
tOE	\overline{OE} to Output Delay		30		40		50	ns	$\overline{CE}=V_{IL}$
tDF	\overline{OE} High to Output Float (Note1)	0	20	0	30	0	30	ns	$\overline{CE}=V_{IL}$
tOH	Address to Output hold	0		0		0		ns	$\overline{CE}=\overline{OE}=V_{IL}$

TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V
- Input rise and fall times: ≤ 10ns
- Output load: 1 TTL gate + 35pF (Including scope and jig)
- Reference levels for measuring timing: 0.8V, 2.0V

NOTE:

- tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

READ TIMING WAVEFORMS


COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION
DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%, VPP = 12V ± 5%

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			1	uA	VIN=GND to VCC
ILO	Output Leakage Current			10	uA	VOUT=GND to VCC
ISB1	Standby VCC current			2	mA	\overline{CE} =VIH
ISB2			1	100	uA	\overline{CE} =VCC ± 0.3V
ICC1 (Read)	Operating VCC Current			40	mA	IOUT=0mA, f=1MHz
ICC2				50	mA	IOUT=0mA, F=10MHz
ICC3 (Program)				50	mA	In Programming
ICC4 (Erase)				50	mA	In Erase
ICCES	VCC Erase Suspend Current			10	mA	\overline{CE} =VIH, Erase Suspended
IPP1 (Read)	VPP Current			200	uA	VPP=12.8V
IPP2 (Program)				50	mA	In Programming
IPP3 (Erase)				50	mA	In Erase
VIL	Input Voltage	-0.3 (Note 5)		0.8	V	
VIH		2.0		VCC+0.3V	V	
				(Note 6)		
VOL	Output Voltage			0.45	V	IOL=2.1mA
VOH		2.4			V	IOH=-400uA
V _{PPLK}	VPP Lockout Voltage	0.0		6	V	
V _{PPH}	VPP for Program	11.4		12.6	V	12V ± 5%

NOTES:

- VCC must be applied before VPP and remove after VPP.
- VPP must not exceed 14V including overshoot.
- An influence may be had upon device reliability if the device is installed or removed while VPP=12V.
- Do not alter VPP either VIL to 12V or 12V to VIL when \overline{CE} =VIL.
- VIL min. = -0.6V for pulse width ≤ 20ns.
- If VIH is over the specified maximum value, programming operation cannot be guaranteed.
- ICCES is specified with the device de-selected. If the device is read during erase suspend mode, current draw is the sum of ICCES and ICC1 or ICC2.
- All current are in RMS unless otherwise noted.

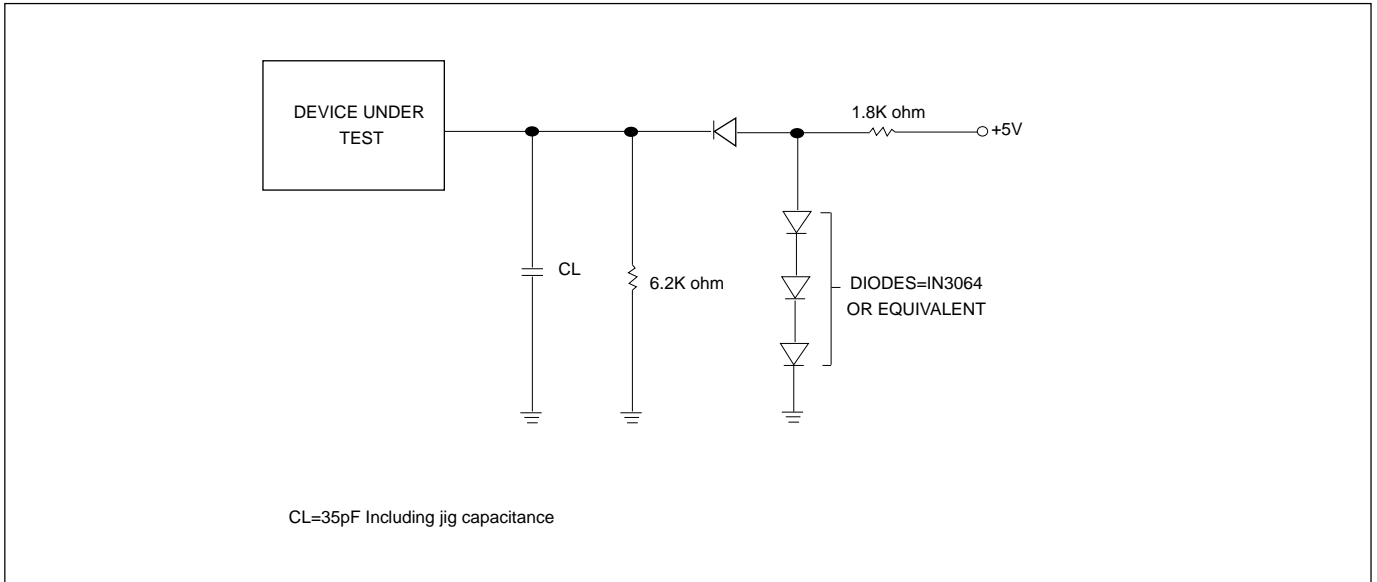
AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%, VPP = 12V ± 5%

SYMBOL	PARAMETER	28F002T/B-70		28F002T/B-90		28F002T/B-12		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
tVPS	VPP setup time	100		100		100		ns	
tPHEL			1000		1000		1000	ns	
tOES	\overline{OE} setup time	100		100		100		ns	
tCWC	Command programming cycle	70		90		120		ns	
tCEP	\overline{WE} programming pulse width	50		50		50		ns	
tCEPH1	\overline{WE} programming pulse width High	20		20		20		ns	
tCEPH2	\overline{WE} programming pulse width High	100		100		100		ns	
tAS	Address setup time	50		50		50		ns	
tAH	Address hold time	10		10		10		ns	
tDS	Data setup time	50		50		50		ns	
tDH	Data hold time	0		0		0		ns	
tCES	\overline{CE} setup time	0		0		0		ns	
tCESC	\overline{CE} setup time before command write	100		100		100		ns	
tCESV	\overline{CE} setup time before verify	6		6		6		us	
tVPH	VPP hold time	100		100		100		ns	
tDF	Output disable time (Note 2)		20		30		30	ns	
tVA	Verify access time		70		90		120	ns	
tAETC	Total erase time in auto erase	5(TYP.)		5(TYP.)		5(TYP.)		s	
tAETB	Total erase time in auto block erase	1(TYP.)		1(TYP.)		1(TYP.)		s	
tAVT	Total programming time in auto verify	50	1600	50	1600	50	1600	us	
tET	Standby time in erase	10		10		10		ms	
tBALC	Block address load cycle	0.3	30	0.3	30	0.3	30	us	
tBAL	Block address load time	100		100		100		us	
tCH	\overline{CE} Hold Time	0		0		0		ns	
tCS	\overline{CE} setup to \overline{WE} going low	0		0		0		ns	

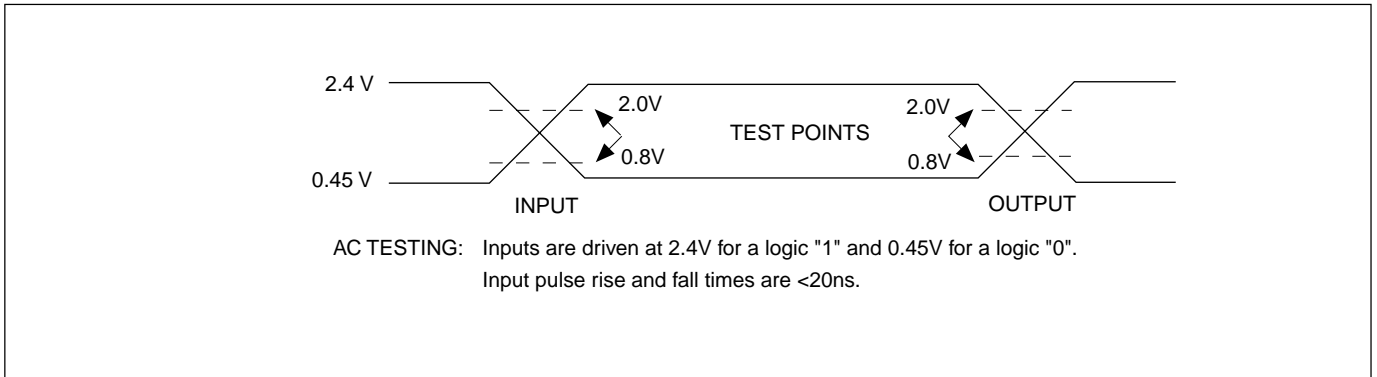
NOTES:

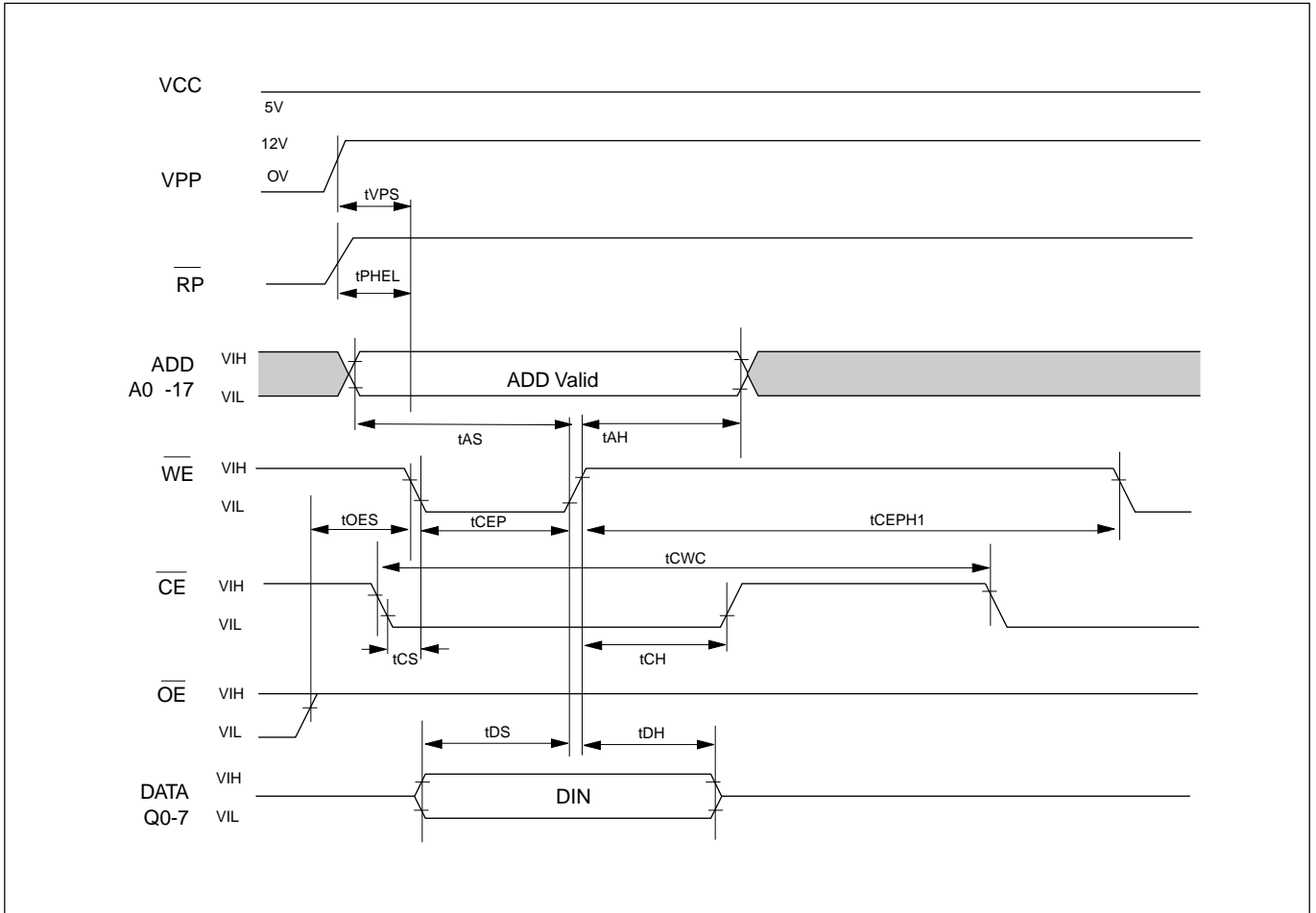
- \overline{CE} and \overline{OE} must be fixed high during VPP transition from 5V to 12V or from 12V to 5V.
- tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.
- tPHEL: \overline{RP} high recovery to \overline{CE} going low: 500ns, Max 1000ns.

SWITCHING TEST CIRCUITS



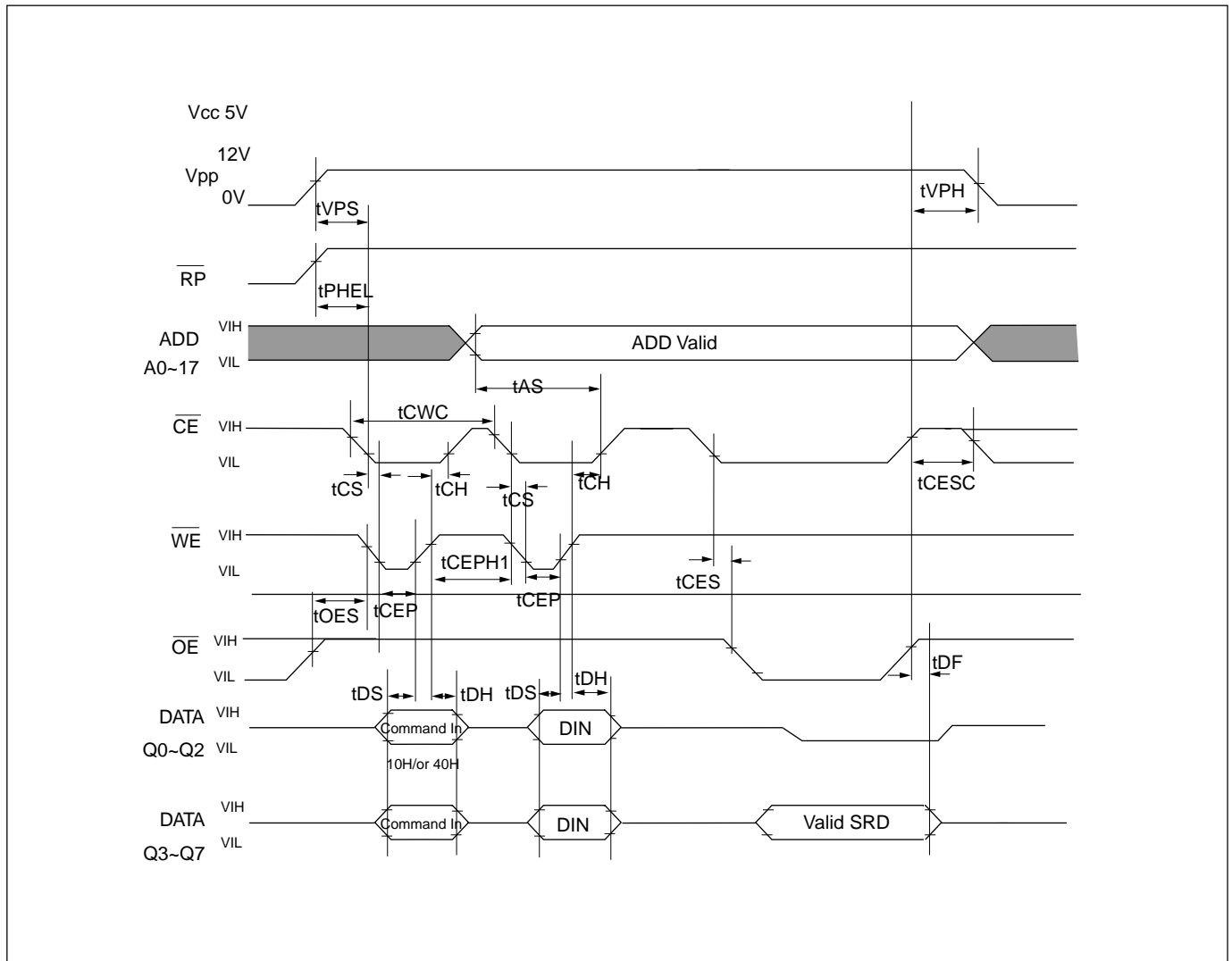
SWITCHING TEST WAVEFORMS

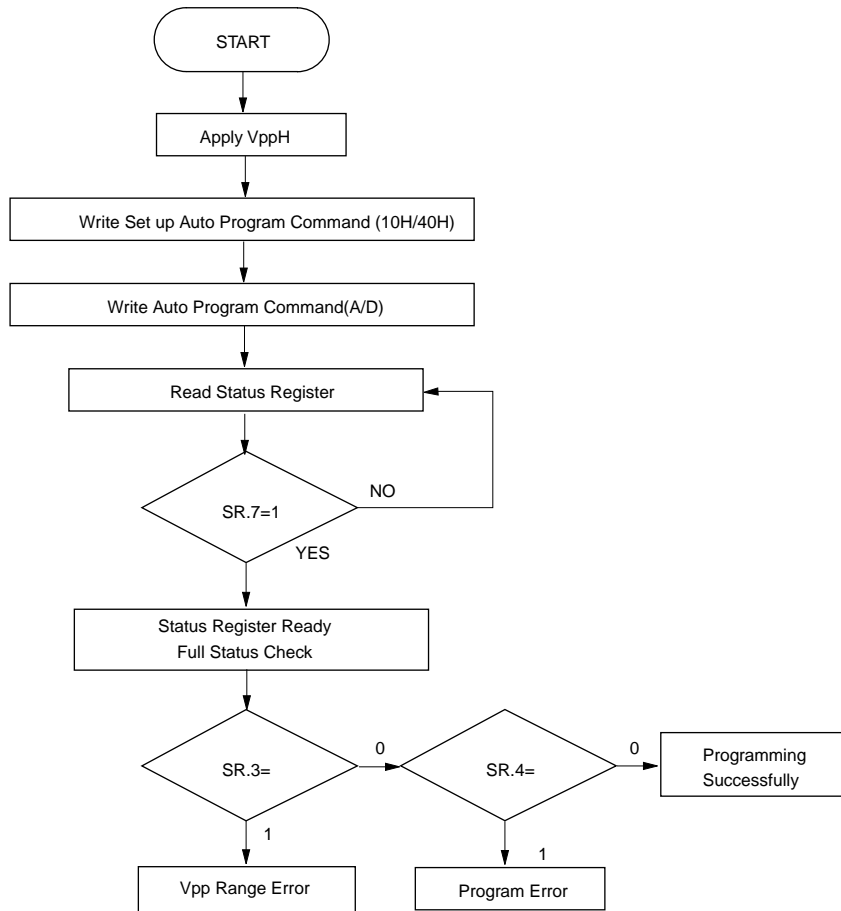


COMMAND WRITE TIMING WAVEFORM


AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional programming by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by status register after automatic Program starts.

AUTOMATIC PROGRAMMING TIMING WAVEFORM


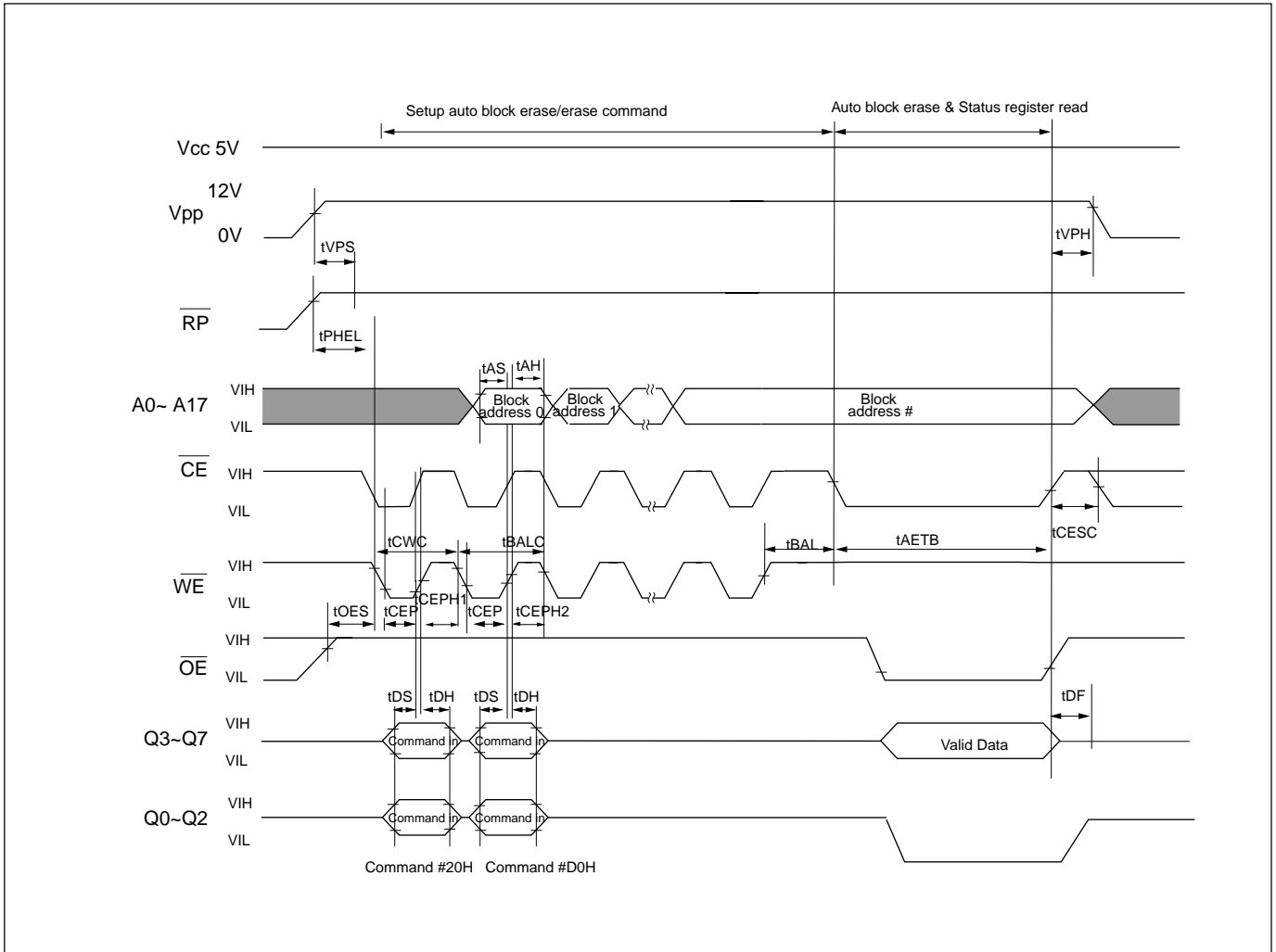
AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART**Program Command Sequence
(Address/Command)**

AUTOMATIC BLOCK ERASE TIMING WAVEFORM

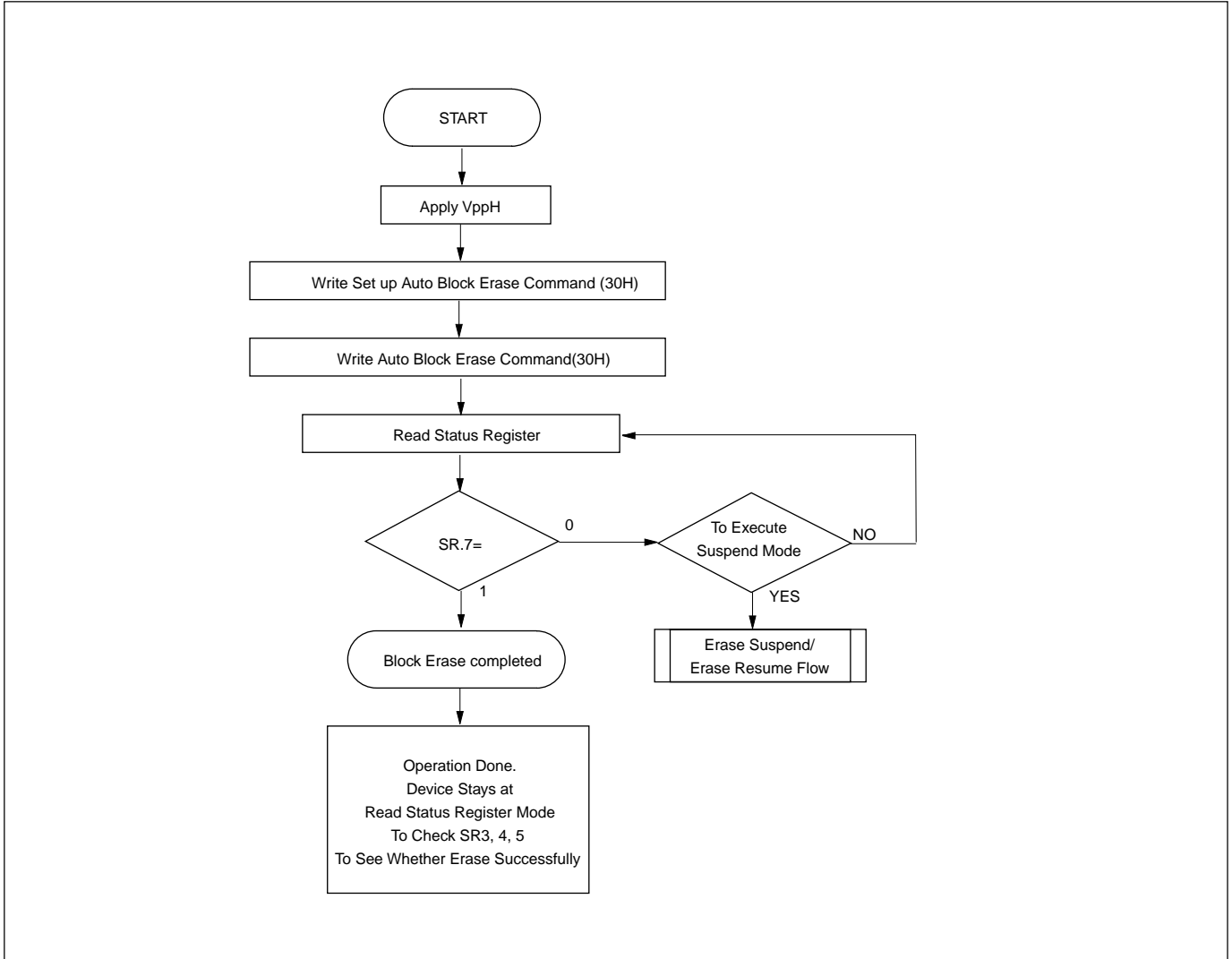
Block data (refer to page 1 for block structure) are erased. External erase verify is not required because data are erased automatically by internal control circuit. Erasure

completion can be verified by status register contents after automatic erase starts.

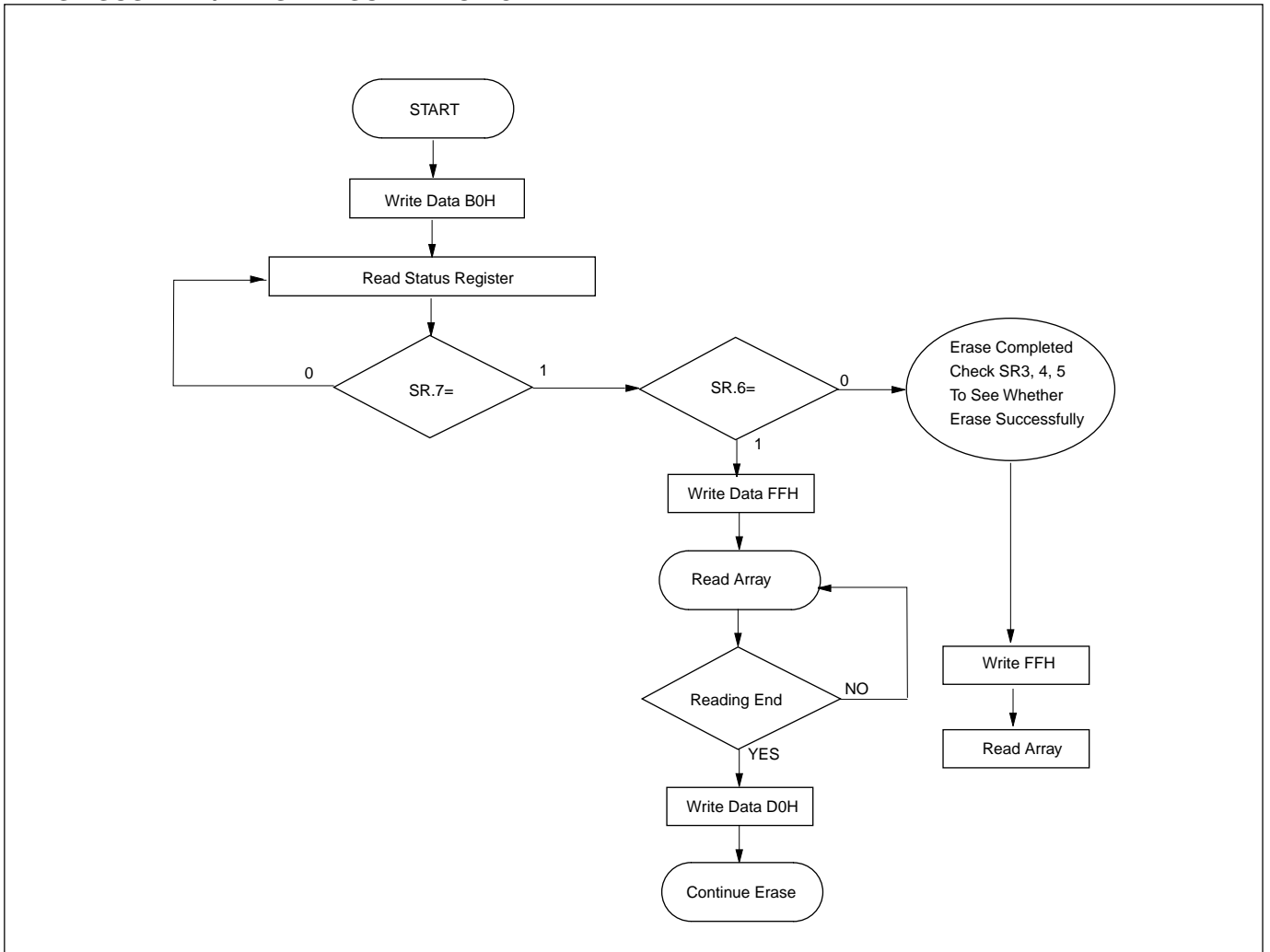
AUTOMATIC BLOCK ERASE TIMING WAVEFORM

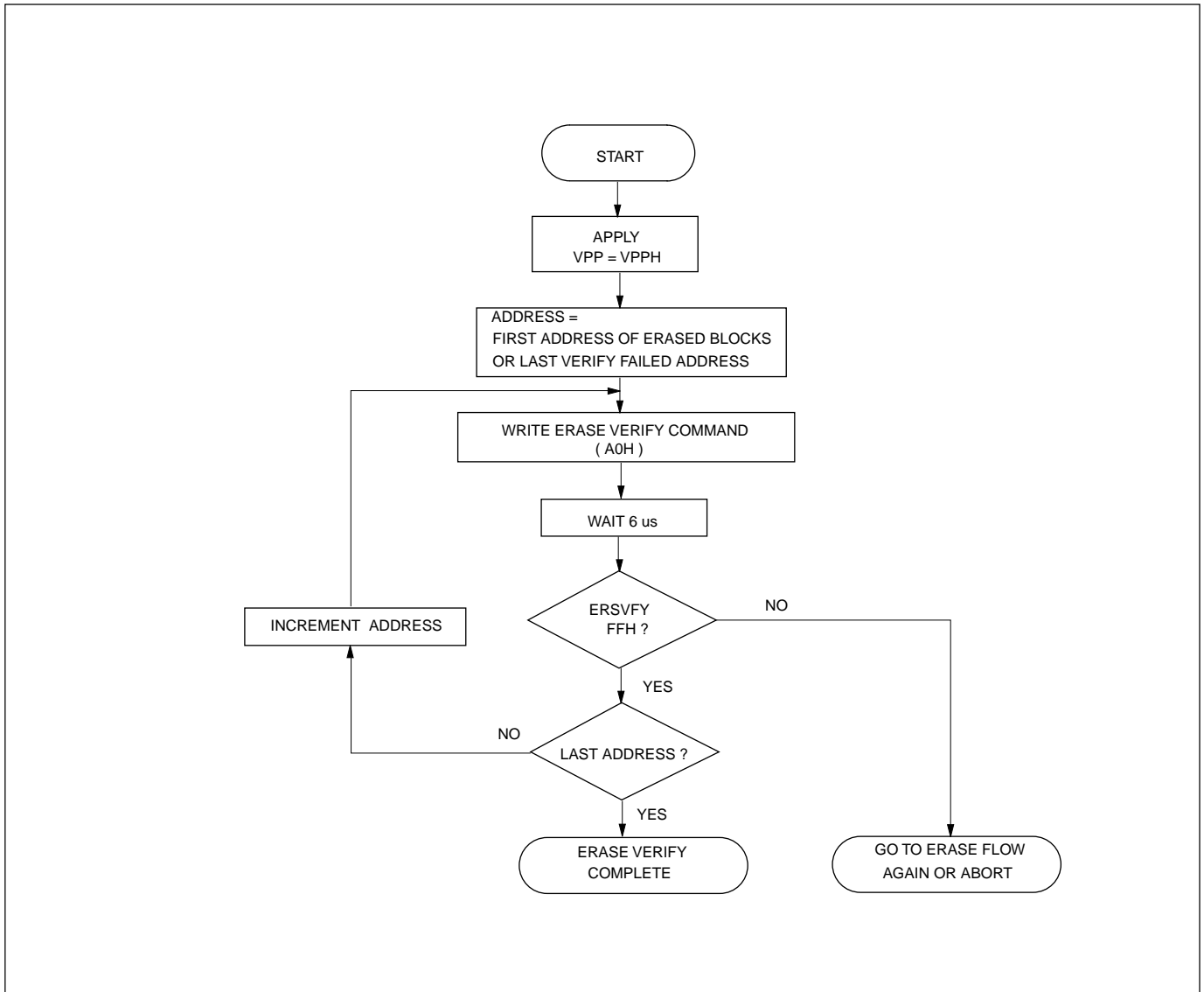


AUTOMATIC BLOCK ERASE ALGORITHM FLOWCHART



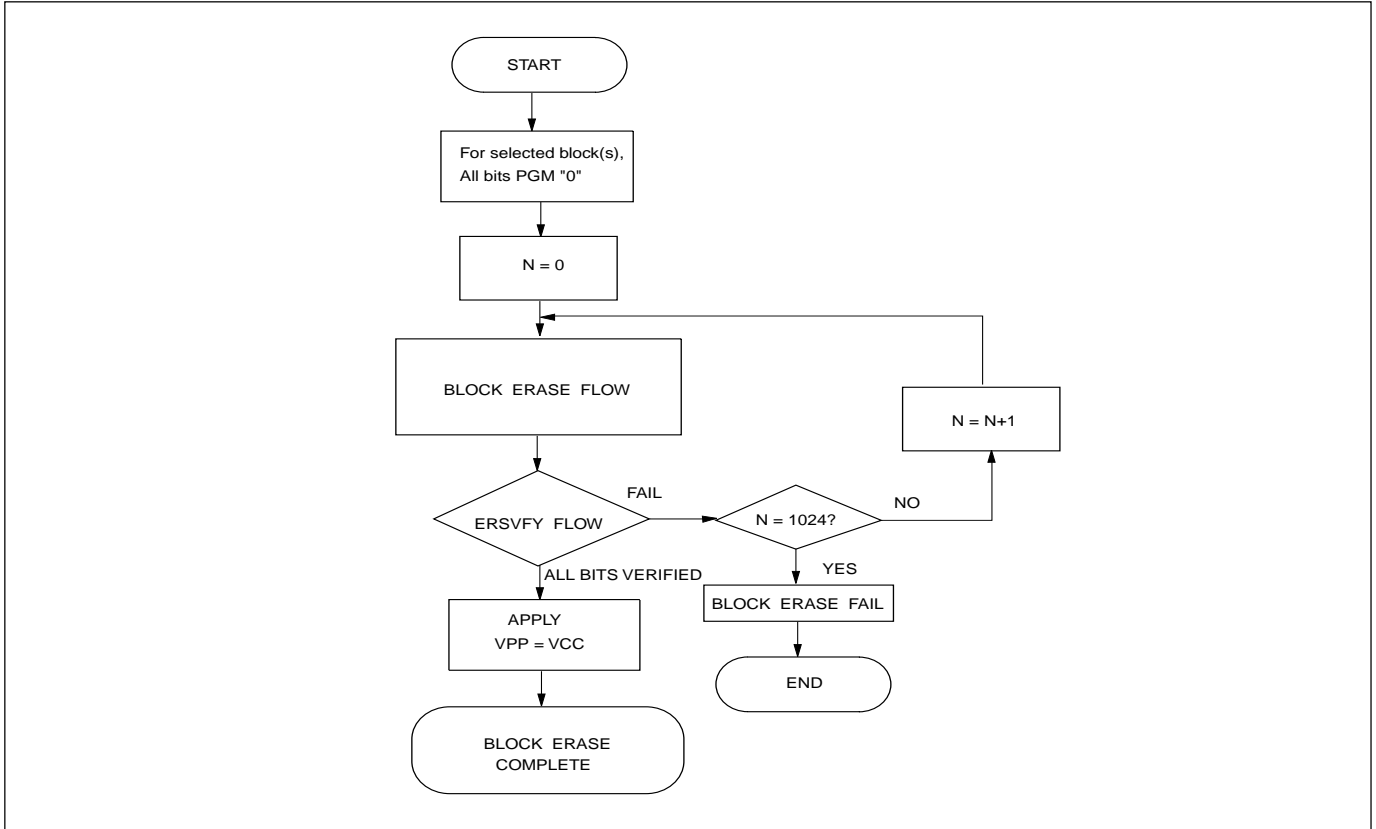
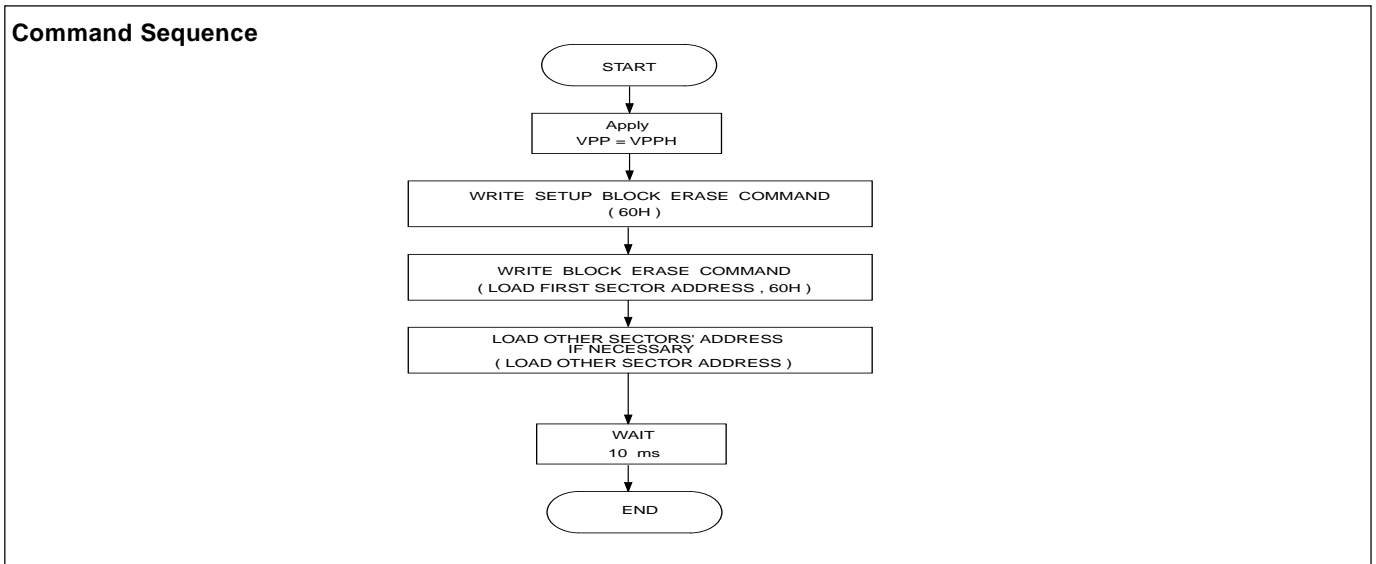
ERASE SUSPEND/ERASE RESUME FLOWCHART

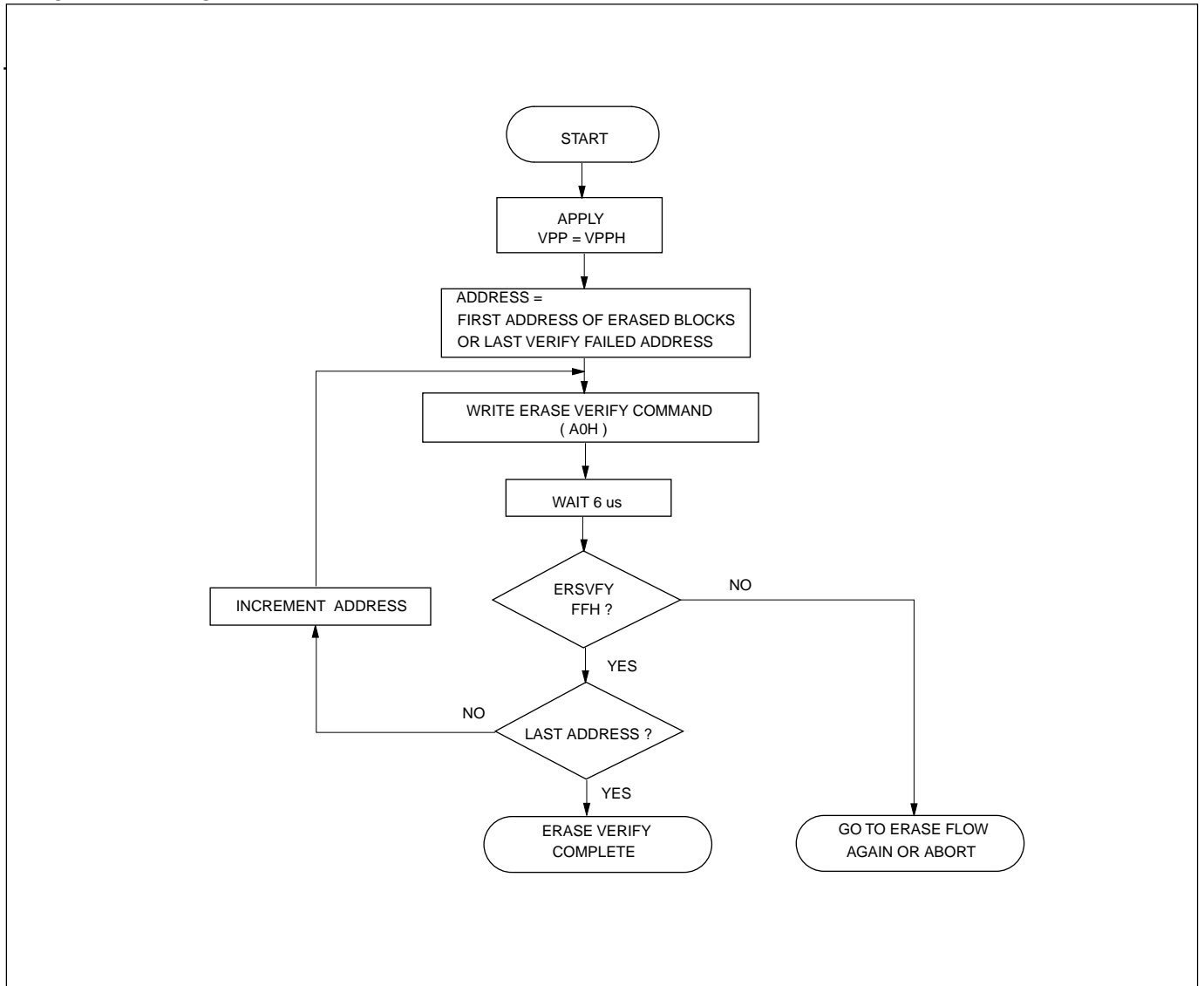


ERASE VERIFY FLOW

FAST HIGH-RELIABILITY BLOCK ERASE

This device can be applied to the fast high-reliability block erase algorithm shown in the following flowchart.

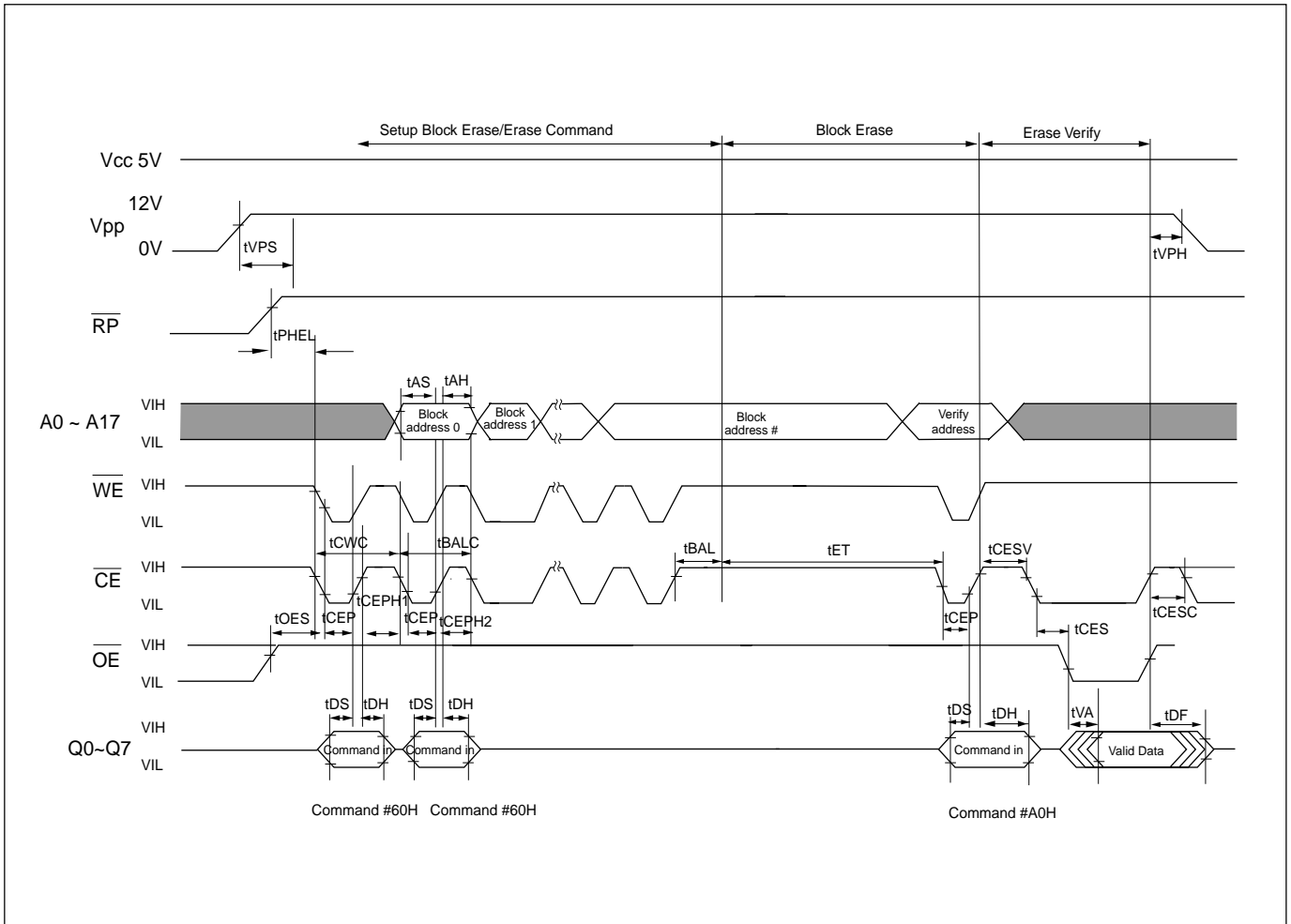
FAST HIGH-RELIABILITY BLOCK ERASE FLOWCHART

BLOCK ERASE FLOW
Command Sequence


ERASE VERIFY FLOW

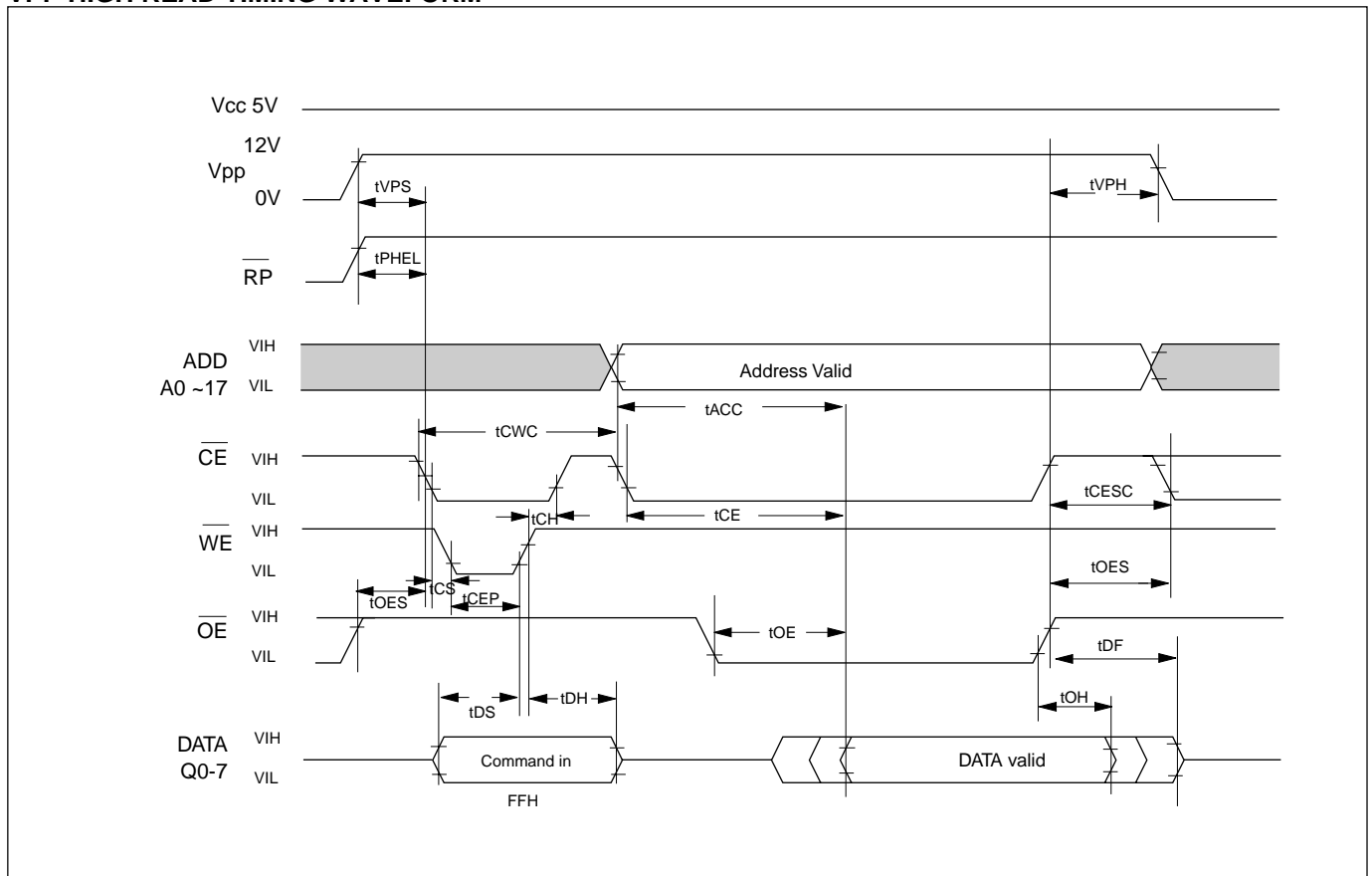
FAST HIGH-RELIABILITY BLOCK ERASE TIMING WAVEFORM

Indicated block data are erased. Control verification and additional erasure externally according to fast high-reliability block erase flowchart.

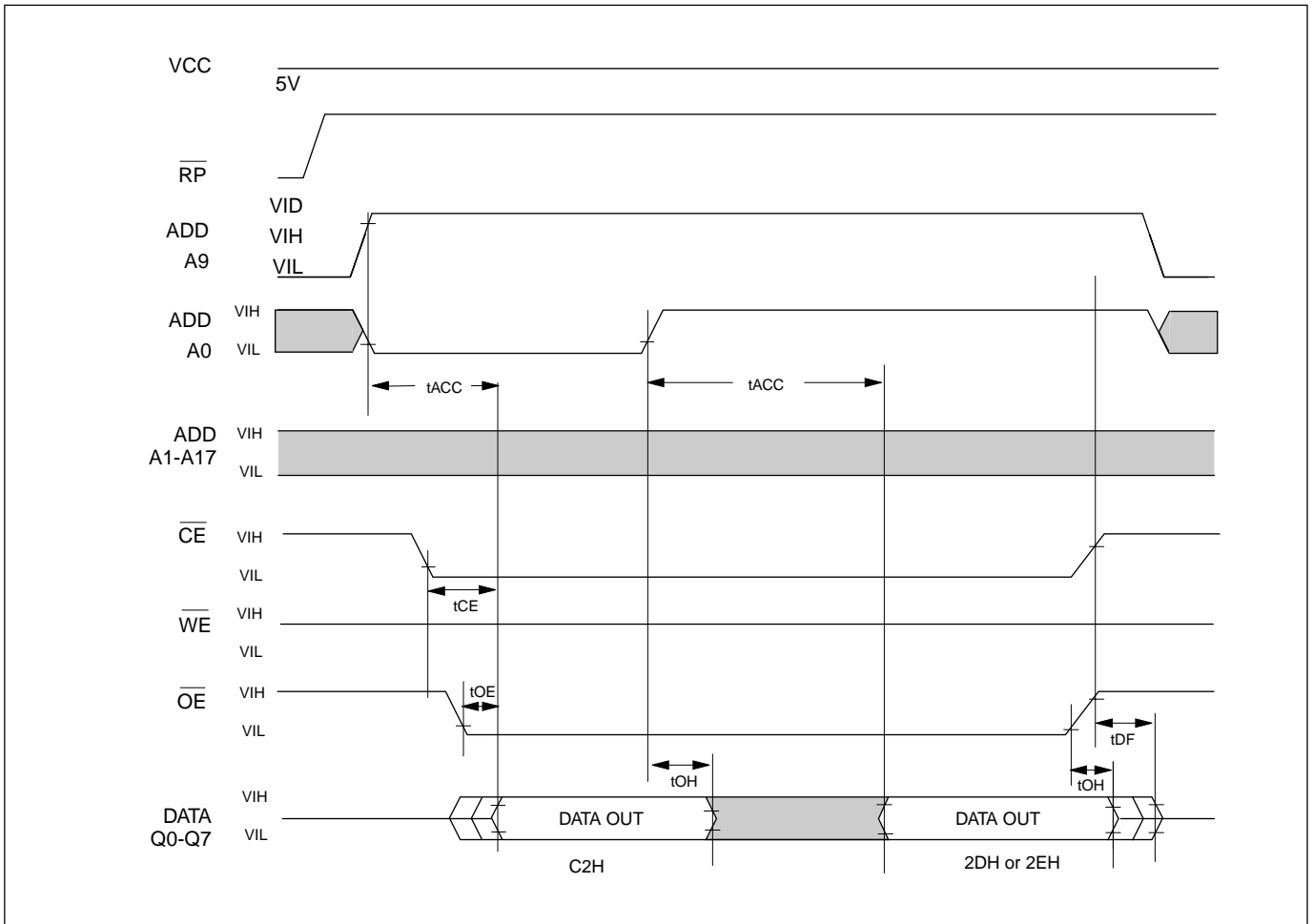
FAST HIGH-RELIABILITY BLOCK ERASE TIMING WAVEFORM



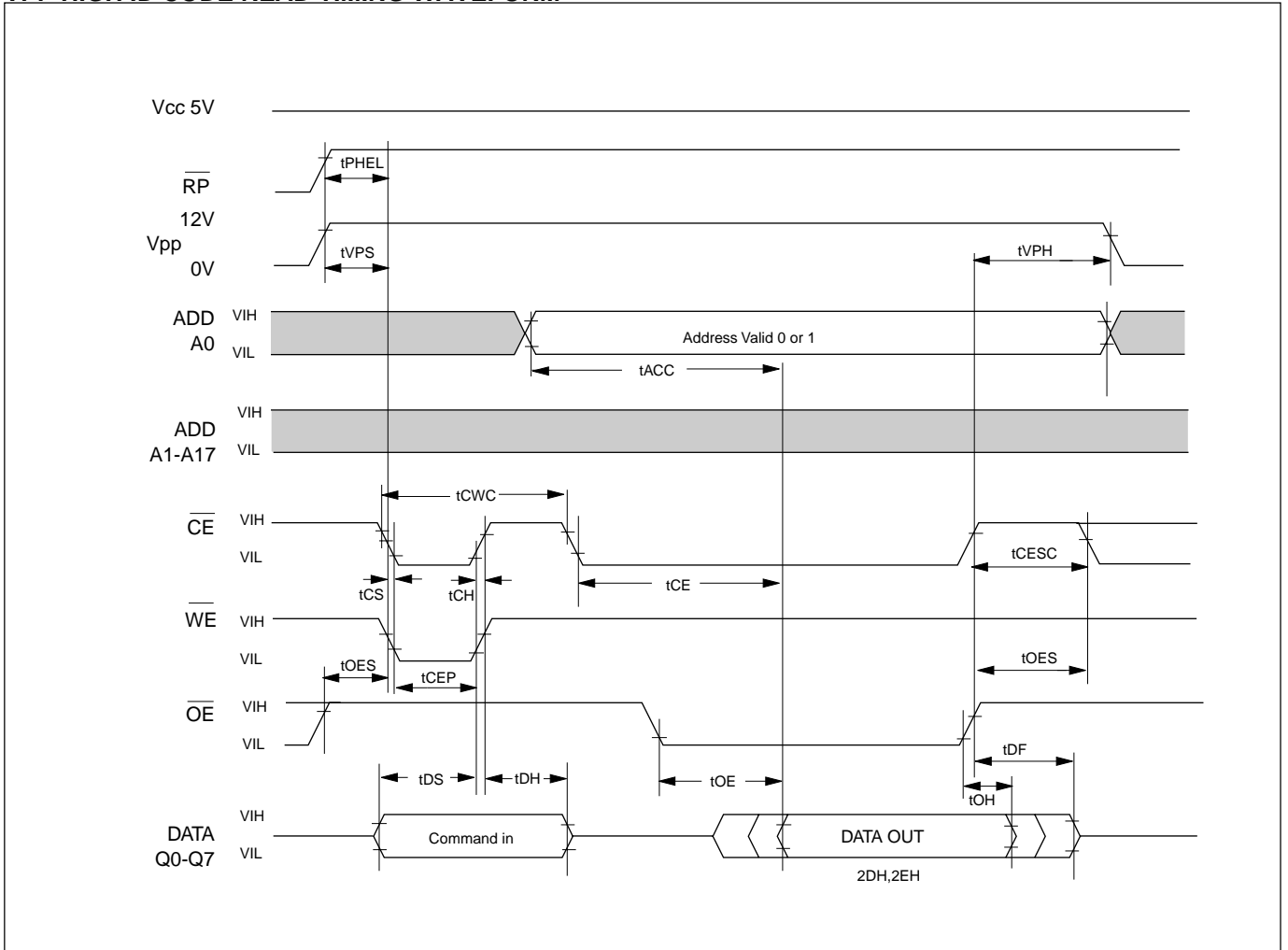
VPP HIGH READ TIMING WAVEFORM



VPP LOW ID CODE READ TIMING WAVEFORM



VPP HIGH ID CODE READ TIMING WAVEFORM



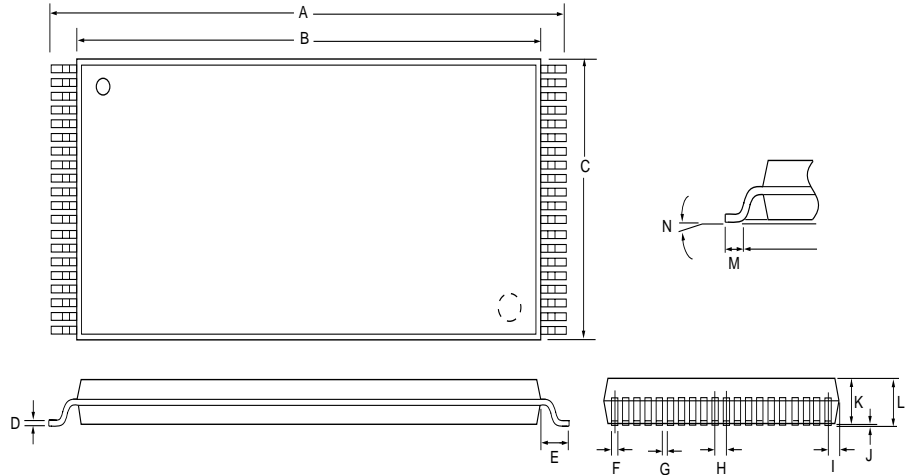
ORDERING INFORMATION**PLASTIC PACKAGE**

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE
MX28F002TTC-70C4	70	50	100	40 Pin TSOP (Normal Type)
MX28F002TTC-90C4	90	50	100	40 Pin TSOP (Normal Type)
MX28F002TTC-12C4	120	50	100	40 Pin TSOP (Normal Type)
MX28F002BTC-70C4	70	50	100	40 Pin TSOP (Normal Type)
MX28F002BTC-90C4	90	50	100	40 Pin TSOP (Normal Type)
MX28F002BTC-12C4	120	50	100	40 Pin TSOP (Normal Type)

PACKAGE INFORMATION

40-PIN PLASTIC TSOP(10mm x 20mm)

ITEM	MILLIMETERS	INCHES
A	20.0 ± .20	.787 ± .008
B	18.40 ± .10	.724 ± .004
C	10.10 max.	.398 max.
D	0.125 [Typ.]	.005 [Typ.]
E	.80 [Typ.]	.031 [Typ.]
F	.20 ± .10	.008 ± .004
G	.30 ± .10	.012 ± .004
H	.50 [Typ.]	.020 [Typ.]
I	.45 max.	.018 max.
J	0 ~ .20	0 ~ .008
K	1.00 ± .10	.039 ± .004
L	1.2 max.	.047 max.
M	.50	.020
N	0 ~ 10°	0 ~ 10°



NOTE: Each lead centerline is located within .25mm [.01 inch] of its true position [TP] at a maximum at maximum material condition.

Revision History

Rev No.	Description	Page	Date
1.1	This product is x8(Byte mode) only. Revise come x 16(Word mode)error.		
1.2	Block erase timing waveform correftion in P20 & P26.		
1.3	Removes "Preliminary".		4/30/1997
1.4	Statement to cleared for customer's better understanding.		10/21/1997
1.6	Add erase time out	P8	Aug/20/1999
1.7	Modify set-up Automatic Block Erase/Erase Command	P8	Aug/23/1999



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