



CAT93C46H

1K BIT SERIAL EEPROM - HIGH ENDURANCE

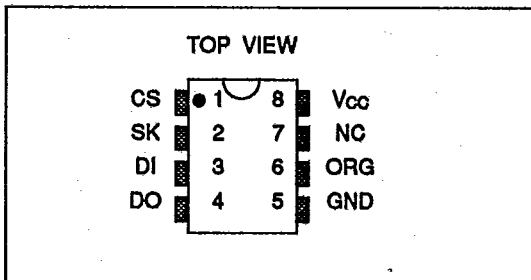
DESCRIPTION

The CAT93C46H is a High Endurance CMOS 1K-bit serial EEPROM with a low current drain of 3 mA active and 100µA standby. Its configuration is user selectable as either 64 registers by 16 bits or 128 registers by 8 bits and has been designed to interface serially with industry standard microcontrollers. Manufactured using Catalyst's advanced CMOS EEPROM floating gate technology, the device can endure 100,000 erase/write cycles and has a data retention of 100 years. The CAT93C46H is assembled in either an 8 pin DIP or S.O. package, and will be available in a 3-volt version (CAT33C101H).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5-volt supply
- 64x16 or 128x8 user selectable serial memory
- Compatible with National Semiconductor NMC 9346
- Self-timed programming cycle with Autoerase
- Word and chip-erasable
- Operating range 0°C to 70°C [industrial temperature range available]
- 100,000 erase/write cycles
- 100 year data retention
- Power-on data protection

PIN CONFIGURATION DIP AND S.O.

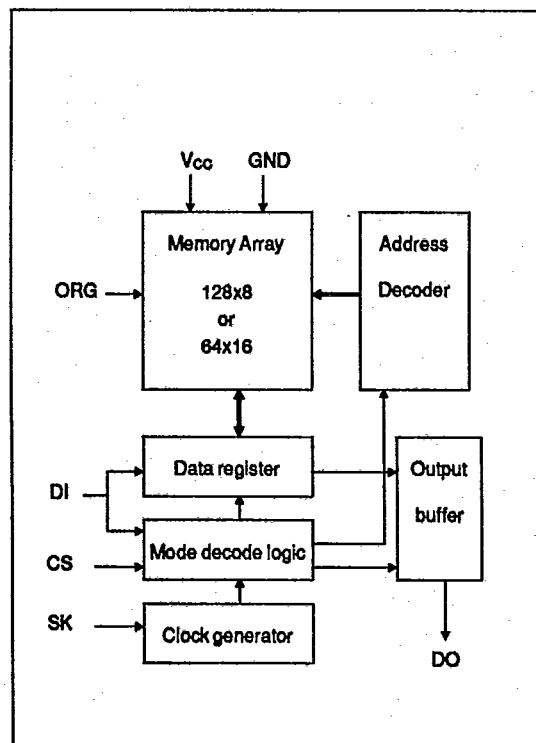


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connect
ORG	Memory organization

Note: - When the ORG pin is connected to +5V, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the ORG pin is left unconnected, an internal pullup device will select the 64x16 organization.

BLOCK DIAGRAM



CAT93C46H

EEPROM

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ABSOLUTE MAXIMUM RATINGS *

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Storage temperature T_{stg} -65°C to +150°C
 Power supply V_{CC} +7 V
 Voltage on any input pin -0.3 to +7V
 Voltage on any output pin -0.3V to $V_{CC} + 0.3V$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

($V_{CC} = +5V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	$V_{CC} = 5.0V$, $CS = V_{IH}$ Outputs unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	$V_{CC} = 5.5V$, $CS = 0V$ $DI = 0V$, $SK = 0V$			100	μA
I_{LI}	Input leakage current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output leakage current	$V_{OUT} = 5.5V$, $CS = 0V$			10	μA
V_{IH}	High level input voltage		2.0		$V_{CC} + 1$	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	$I_{OH} = -400\mu A$	2.4			V
V_{OL}	Low level output voltage	$I_{OL} = 2.1mA$			0.4	V

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1 0	A6 - A0	A5 - A0			Read address AN - A0
ERASE	1	1 1	A6 - A0	A5 - A0			ERASE address AN - A0
WRITE	1	0 1	A6 - A0	A5 - A0	D7 - D0	D15 - D0	WRITE address AN - A0
EWEN	1	0 0	11XXXXX	11XXXX			Program enable
EWDS	1	0 0	00XXXXX	00XXXX			Program disable
ERAL	1	0 0	10XXXXX	10XXXX			Erase all addresses
WRAL	1	0 0	01XXXXX	01XXXX	D7 - D0	D15 - D0	Program all addresses

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AC CHARACTERISTICS

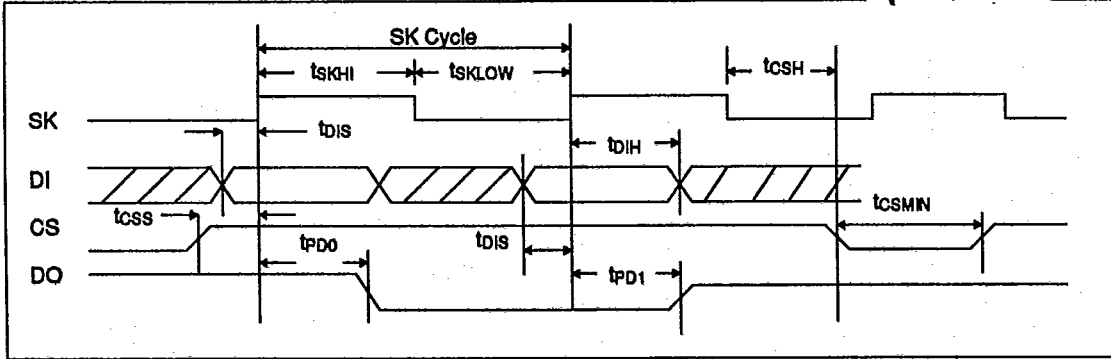
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(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{CSS}	CS setup time		0.2			μs
t _{CSH}	CS hold time	C _L = 100pF V _{OL} = 0.8V, V _{OH} = 2.0V V _{IL} = 0.45V, V _{IH} = 2.4V	0			μs
t _{DIS}	DI setup time		0.4			μs
t _{DIH}	DI hold time		0.4			μs
t _{PD1}	Output delay to 1				2	μs
t _{PD0}	Output delay to 0			2	μs	
t _{HZ}	Output delay to Hi-Z			0.4	μs	
t _{EW}	Erase/Write pulse width			10	ms	
t _{CSMIN}	Minimum CS low time		1		μs	
t _{SKHI}	Minimum SK high time		1		μs	
t _{SKLOW}	Minimum SK low time		1		μs	
t _{SV}	Output delay to status valid	C _L = 100pF			1	μs
SK _{MAX}	Maximum frequency		DC		250	kHz

SYNCHRONOUS TIMINGS

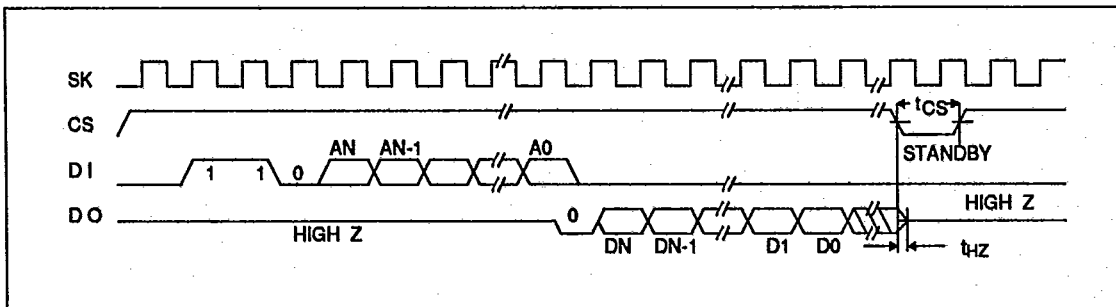
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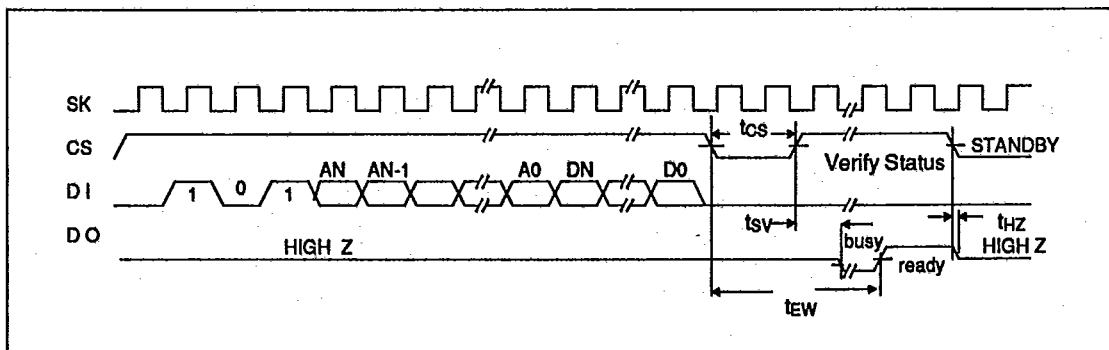
INSTRUCTION TIMING <ORGANIZATION>

Organization	A _N (or AN)	D _N (or DN)
128 x 8	A ₆	D ₇
64 x 16	A ₅	D ₁₅

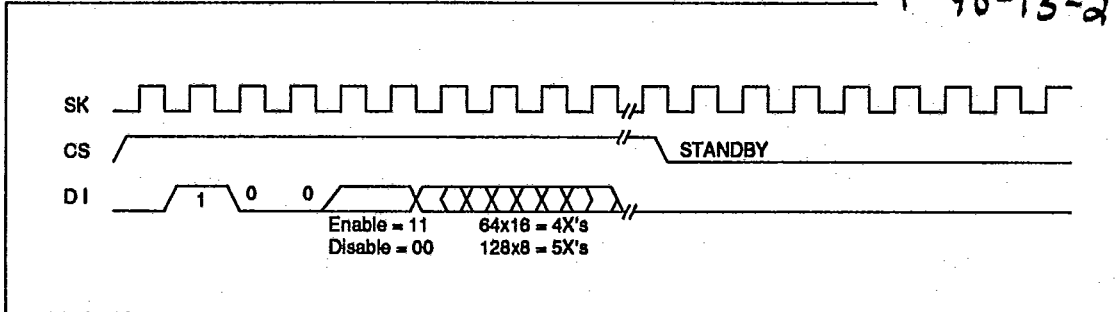
INSTRUCTION TIMING <READ>



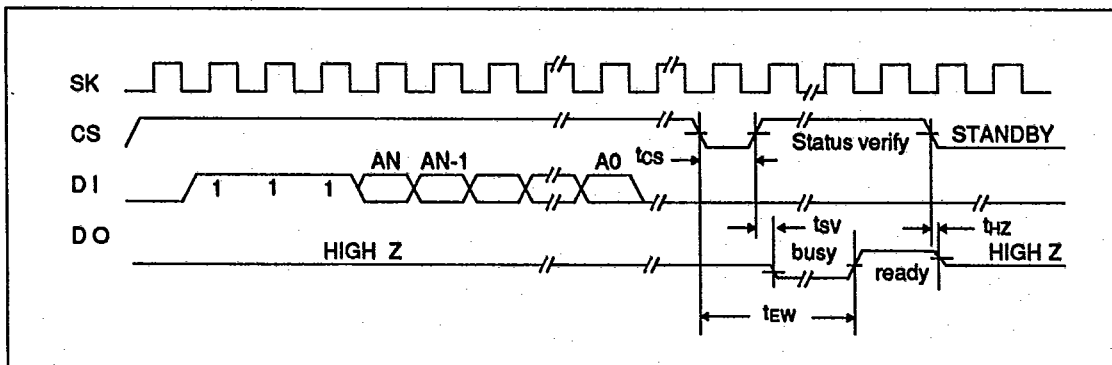
INSTRUCTION TIMING <WRITE>



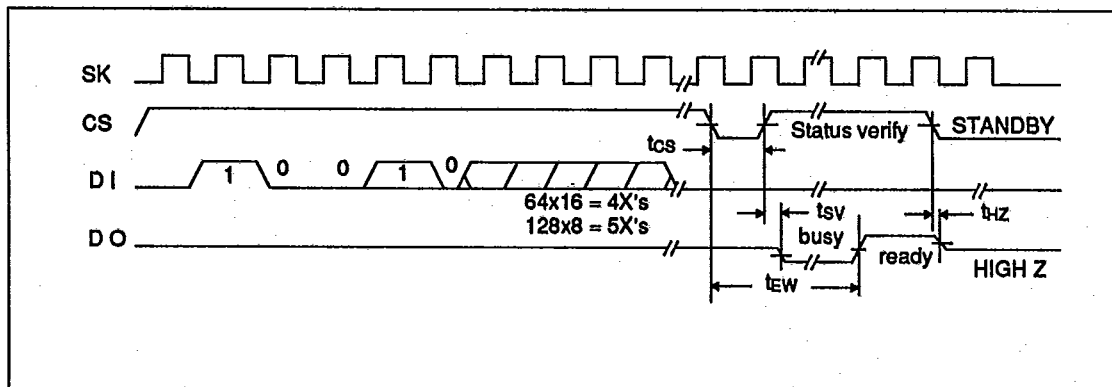
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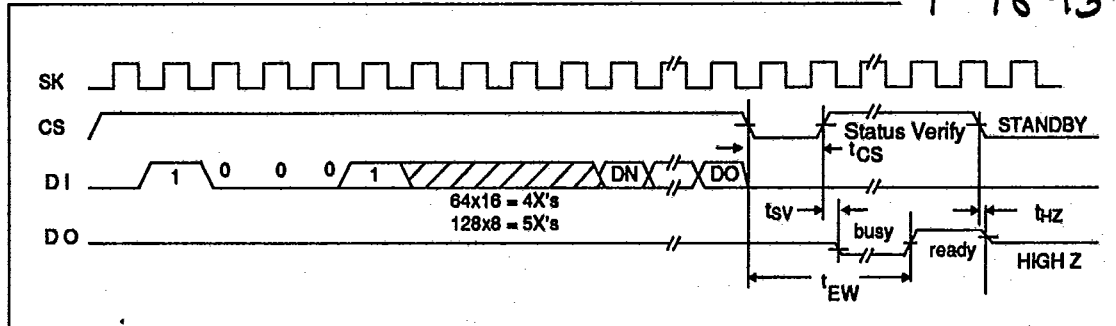
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



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DEVICE OPERATION

The CAT93C46H is a 1024 bit non-volatile memory intended for use with the COPS™ family of microcontrollers, or other standard microprocessors. The CAT93C46H can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Seven 9-bit instructions (10-bit instructions in 128 by 8 organization) control the reading, writing, and erase operations of the device. The CAT93C46H operates on a single 5-Volt supply and will generate on-chip the high voltage required during any programming operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT93C46H is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46H will come out of the high impedance state, and after sending an initial dummy zero bit, will begin shifting out the 16 (or 8) bits of data located at the specified address. The data bits being shifted out will toggle on the rising edge of the SK clock and are stable after the specified time delay t_{PD0} or t_{PD1} .

ERASE/WRITE ENABLE AND DISABLE

The CAT93C46H powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46H programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT93C46H regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the device must be deselected for a minimum of 1 μ s (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of

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the CAT93C46H can be determined by selecting the device and polling the DO pin.

device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46H can be determined by selecting the device and polling the DO pin.

WRITE

After receiving a WRITE command, address and data, the device must be deselected for a minimum of 1 μs (TcSMIN). The falling edge of CS will start the self clocking erase and data store cycle of the memory register specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46H can be determined by selecting the device and polling the DO pin. With the CAT93C46H it is NOT necessary to erase a memory register before the WRITE command.

WRITE ALL

Upon receiving a WRITE ALL command and data, the device must be deselected for a minimum of 1 μs (TcSMIN). The falling edge of CS will start the self clocking write cycle to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46H can be determined by selecting the device and polling the DO pin.

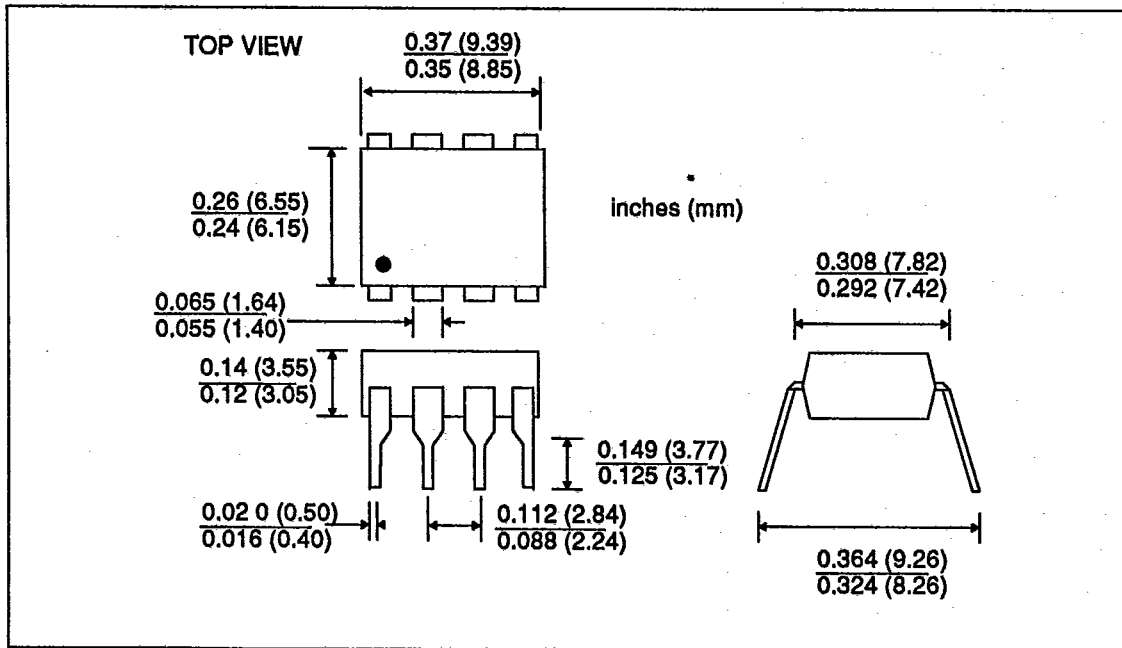
ERASE ALL

Upon receiving an ERASE ALL command, the device must be deselected for a minimum of 1 μs (TcSMIN). The falling edge of CS will start the self clocking erase cycle of all memory locations in the

It IS necessary for all memory locations to be erased before the WRITE ALL command is executed.

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PACKAGE DIAGRAM <8 PIN-DIP>



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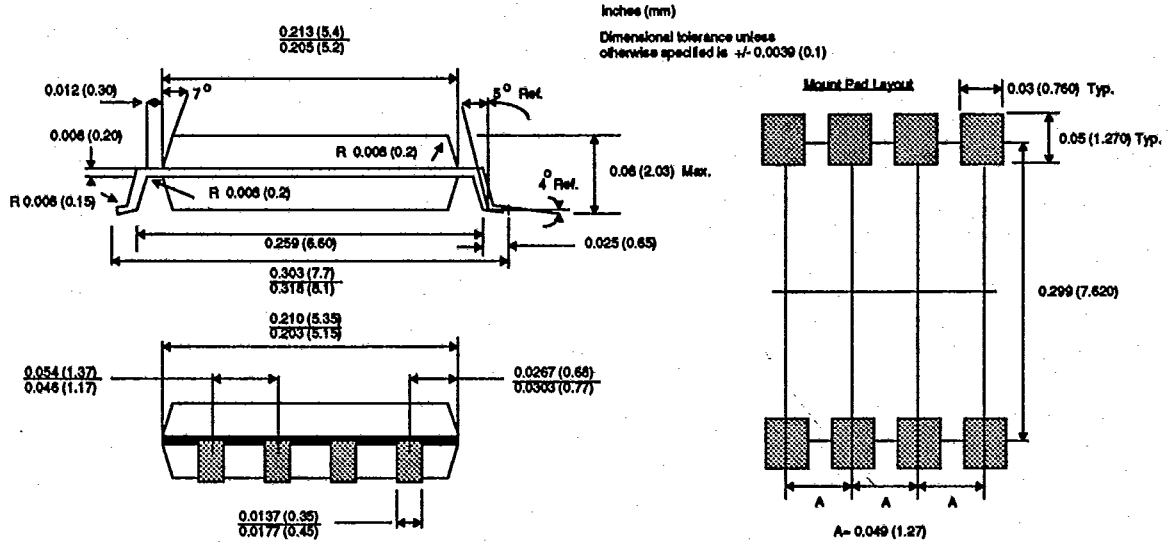
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PACKAGE DIAGRAM <8 Pin Small Outline>



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