

CAT93C46AH - High Endurance 1K BIT SERIAL E²PROM

700KHz OPERATION

DESCRIPTION

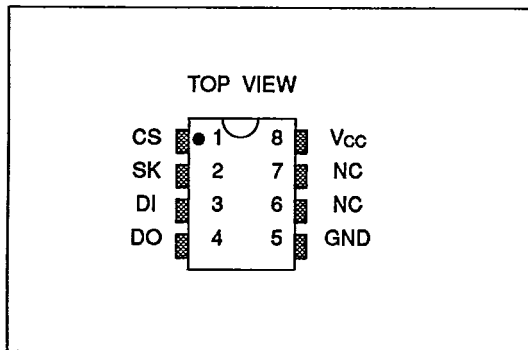
The CAT93C46AH is an industrial temperature CMOS 1K-bit serial E²PROM with a low current drain of 3mA active and 100µA standby. It is configured as 64 registers of 16 bits each, and has been designed to interface serially with industry standard microcontrollers. Manufactured using Catalyst's advanced CMOS E²PROM floating gate technology, the device can endure 100,000 erase/write cycles and has a data retention of 100 years. The CAT93C46AH is assembled in either an 8 pin DIP or S.O. package, and will be available in a 3V version (CAT33C101AH).

FEATURES

- High-speed 700KHz operation
- Single 5V supply
- 64x16 serial memory
- Compatible with National Semiconductor NMC 9346
- Self-timed programming cycle with Autoerase
- Word and chip-erasable
- Operating range 0°C to +70°C
- Highly reliable CMOS floating gate technology
- 100,000 erase/write cycles
- 100 year data retention
- Power-up inadvertent write protection



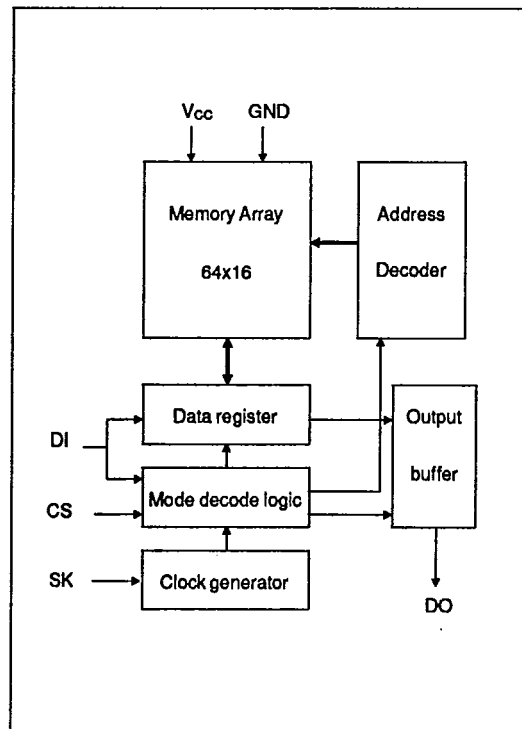
PIN CONFIGURATION DIP AND S.O.



PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connect

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS *

Storage temperature	-65°C to +150°C
Power supply (V _{CC})	+7V
Voltage on any input pin	-0.3 to +7V
Voltage on any output pin	-0.3V to V _{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{CC1}	Current consumption (operating)	DI = 0.0V, SK = 5.0V V _{CC} = 5.0V, CS = 5.0V Outputs unloaded			3	mA
I _{CC2}	Current consumption (stand-by)	V _{CC} = 5.5V, CS = 0V DI = 0V, SK = 0V			100	µA
I _{LI}	Input leakage current	V _{IN} = 5.5V			10	µA
I _{LO}	Output leakage current	V _{OUT} = 5.5V, CS = 0V			10	µA
V _{IH}	High level input voltage		2.0		V _{CC} + 1	V
V _{IL}	Low level input voltage		-0.1		0.8	V
V _{OH}	High level output voltage	I _{OH} = -400µA	2.4			V
V _{OL}	Low level output voltage	I _{OL} = 2.1mA			0.4	V

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address	Data	Comments
READ	1	1 0	A5 - A0		Read address AN - A0
ERASE	1	1 1	A5 - A0		Erase address AN - A0
WRITE	1	0 1	A5 - A0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXX		Program enable
EWDS	1	0 0	00XXXX		Program disable
ERAL	1	0 0	10XXXX		Erase all addresses
WRAL	1	0 0	01XXXX	D15 - D0	Program all addresses

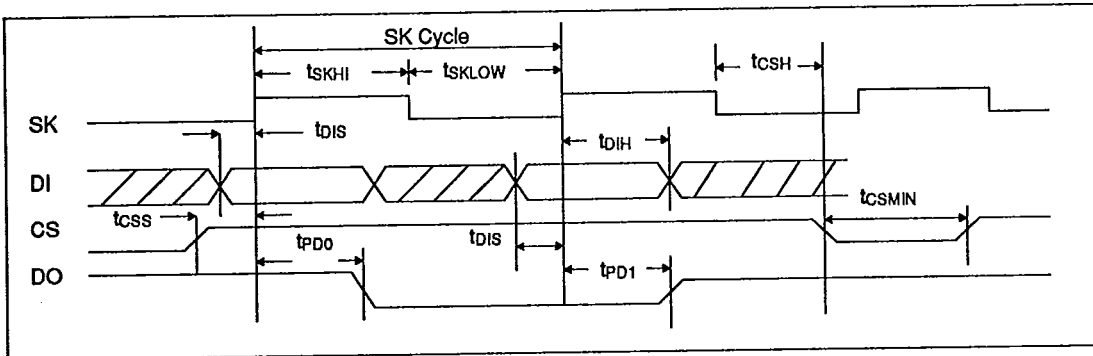
AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

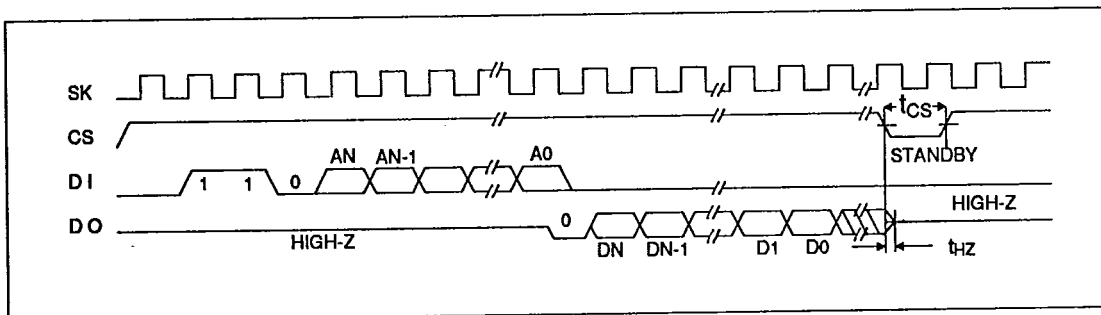
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{CS}	CS setup time		50			ns
t _{CSH}	CS hold time	C _L = 100pF V _{OL} = 0.8V, V _{OH} = 2.0V V _{IL} = 0.45V, V _{IH} = 2.4V	0			ns
t _{DIS}	DI setup time		100			ns
t _{DIH}	DI hold time		100			ns
t _{PD1}	Output delay to 1				500	ns
t _{PD0}	Output delay to 0				500	ns
t _{HZ}	Output delay to Hi-Z				100	ns
t _{EW}	Erase/Write pulse width			10	ms	
t _{CSMIN}	Minimum CS low time		250		ns	
t _{SKHI}	Minimum SK high time		100		ns	
t _{SKLOW}	Minimum SK low time		660		ns	
t _{SV}	Output delay to status valid	C _L = 100pF			500	ns
SK _{MAX}	Maximum clock frequency		DC		700	kHz



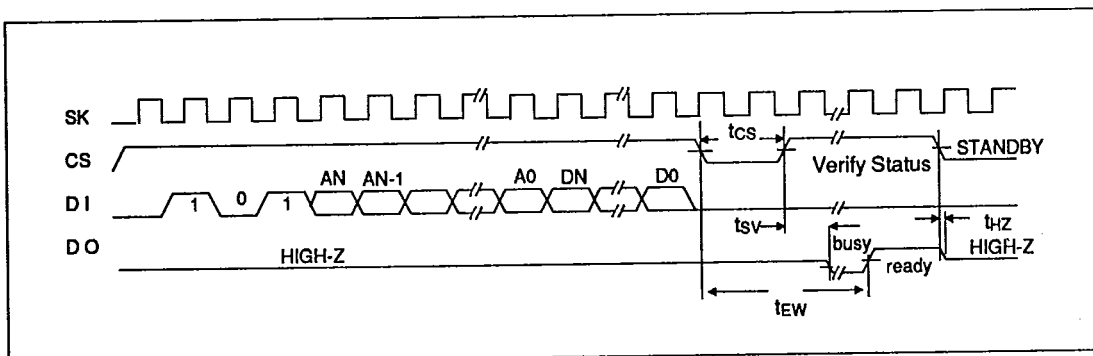
SYNCHRONOUS TIMINGS



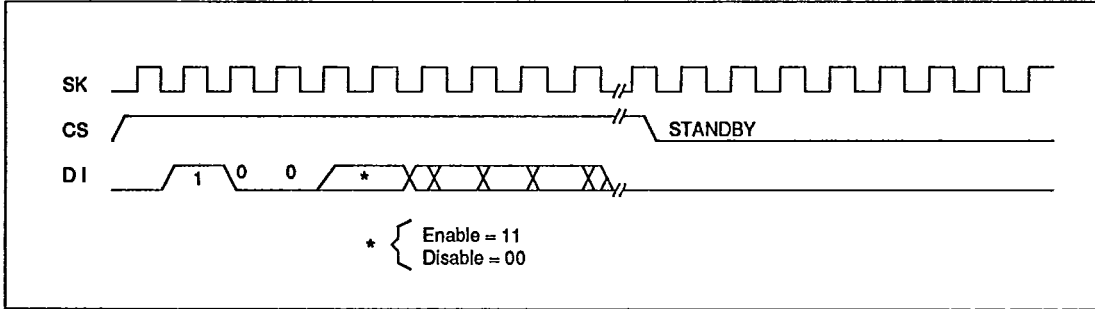
INSTRUCTION TIMING <READ>



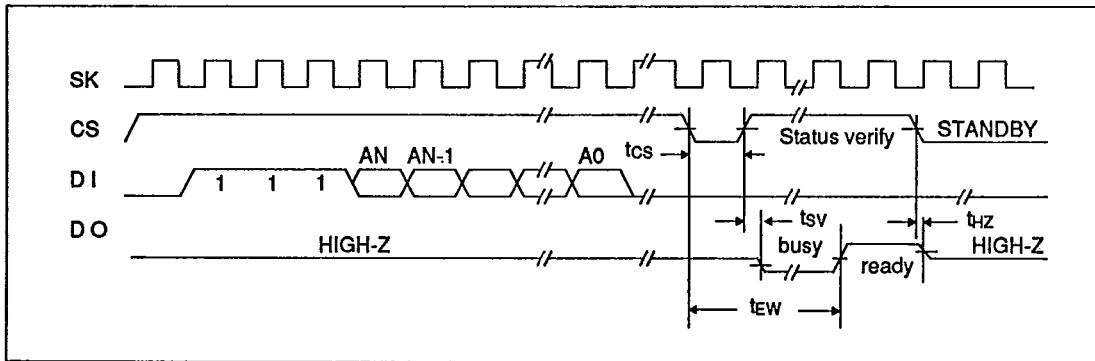
INSTRUCTION TIMING <WRITE>



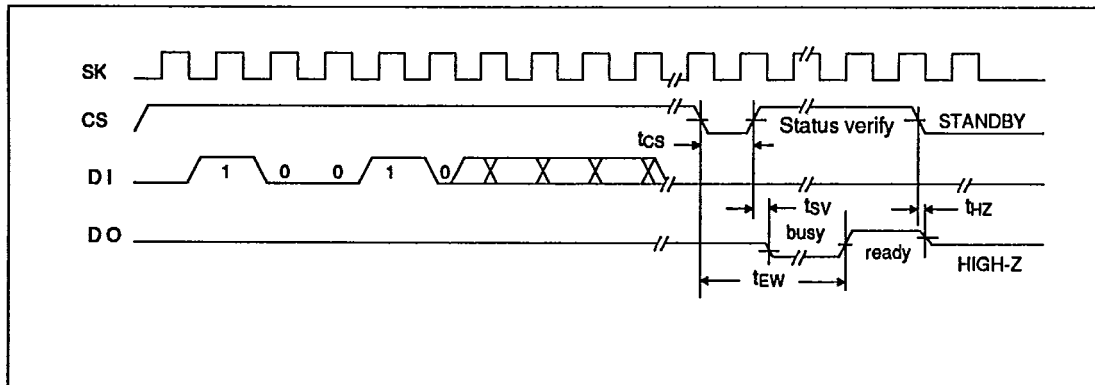
INSTRUCTION TIMING <EWEN, EWDS>



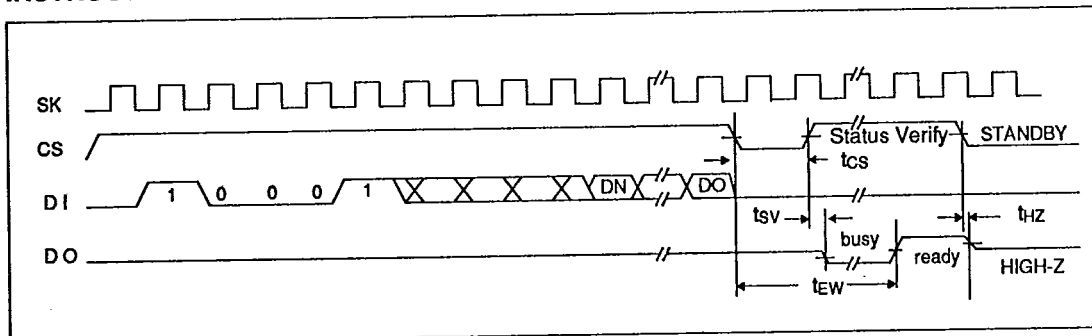
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT93C46AH is a 1024 bit nonvolatile memory intended for use with the COPS™ family of microcontrollers and designed to operate smoothly with other standard microprocessors as well. The CAT93C46AH is organized as 64 registers by 16 bits. Seven 9 bit instructions control the reading, writing and erase operations of the device. The CAT93C46AH fully operates on a single 5V supply including the programming operation. Instructions, addresses and data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin remains in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT93C46AH is a logical "1" start bit, a 2 bit op code, a 6 bit address, and for write operations, a 16 bit data field.

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46AH will come out of the high impedance state, and after sending an initial dummy zero bit,

will begin shifting out the 16 bits of data located at the specified address. The data bits being shifted out will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} and t_{PD1}).

ERASE/WRITE ENABLE AND DISABLE

The CAT93C46AH powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46AH programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT93C46AH regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46AH can be determined by selecting the device and polling the DO pin. Once erased, all memory locations return to a logical "1" state.

WRITE

After receiving a WRITE command, address and data, the device must be deselected for a minimum



of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory register specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46AH can be determined by selecting the device and polling the DO pin. With the CAT93C46AH it is **NOT** necessary to erase a memory register before the WRITE command.

ERASE ALL

Upon receiving an ERAL command, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46AH can be determined by selecting the device and polling the

DO pin. Once erased, all memory locations return to logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking write cycle to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46AH can be determined by selecting the device and polling the DO pin.

It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

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