

# CAT33C108/CAT33C108I

8K-Bit SERIAL E<sup>2</sup>PROM

## FEATURES

- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Single 3V Supply
- 512 x 16 or 1024 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Sequential Read
- Program Enable (PE) Pin
- Fast Nonvolatile Write Cycle: 5ms Max
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

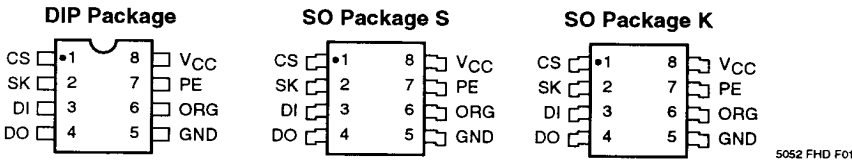
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## DESCRIPTION

The CAT33C108 and CAT33C108I are 8K bit Serial E<sup>2</sup>PROM memory devices which can be configured as either 512 registers by 16 bits (ORG pin at V<sub>CC</sub>) or 1024 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin.

The CAT33C108/CAT33C108I is manufactured using Catalyst's advanced CMOS E<sup>2</sup>PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

## PIN CONFIGURATION

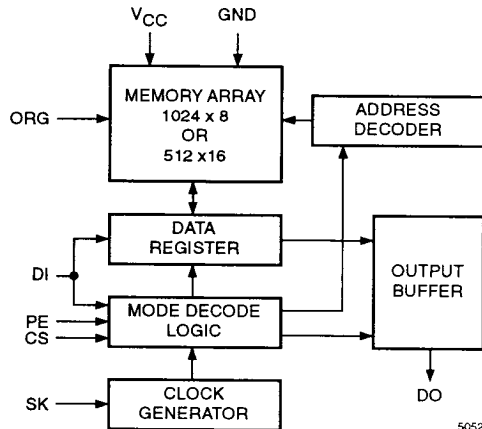


## PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V <sub>CC</sub>	+3V Power Supply
GND	Ground
PE	Program Enable
ORG	Memory Organization

Note: When the ORG pin is connected to V<sub>CC</sub>, the 512 x 16 organization is selected. When it is connected to ground, the 1024 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 512 x 16 organization.

## BLOCK DIAGRAM



5052 FHD F02  
TD 5052

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias .....-55°C to +125°C  
 Storage Temperature .....-65°C to +150°C  
 Voltage on any Pin with  
     Respect to Ground<sup>(1)</sup> .....-2.0V to +V<sub>CC</sub> +2.0V  
 V<sub>CC</sub> with Respect to Ground .....-2.0V to +7.0V  
 Package Power Dissipation  
     Capability (T<sub>a</sub> = 25°C) ..... 1.0W  
 Lead Soldering Temperature (10 secs) ..... 300°C  
 Output Short Circuit Current<sup>(2)</sup> ..... 100 mA

**\*COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

**RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N <sub>END</sub> <sup>(3)</sup>	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T <sub>DR</sub> <sup>(3)</sup>	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V <sub>ZAP</sub> <sup>(3)</sup>	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I <sub>LTH</sub> <sup>(3)(4)</sup>	Latch-Up	100		mA	JEDEC Standard 17

**D.C. OPERATING CHARACTERISTICS**

CAT33C108 T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = +3V±10%, unless otherwise specified.  
 CAT33C108I T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = +3V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I <sub>CC1</sub>	Power Supply Current (Operating)	Comm.		2	mA	DI = 0.0V, SK = 3.0V V <sub>CC</sub> = 3.0V, CS = 3.0V, Output Open
		Ind.		3	mA	
I <sub>CC2</sub>	Power Supply Current (Standby)			10	µA	V <sub>CC</sub> = 3.3V, CS = 0V DI = 0V SK = 0V
I <sub>LI</sub> <sup>(5)</sup>	Input Leakage Current			1	µA	V <sub>IN</sub> = 0V to 3.3V
I <sub>LO</sub> <sup>(5)</sup>	Output Leakage Current (Including ORG Pin)			1	µA	V <sub>OUT</sub> = 0V to 3.3V, CS = 0V
V <sub>IH</sub>	High Level Input Voltage	V <sub>CC</sub> - 0.3		V <sub>CC</sub> + 1	V	
V <sub>IL</sub>	Low Level Input Voltage	-0.1		0.3	V	
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> - 0.3			V	I <sub>OH</sub> = -10µA
V <sub>OL</sub>	Low Level Output Voltage			0.3	V	I <sub>OL</sub> = 10µA

Note:

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> +0.5V, which may overshoot to V<sub>CC</sub> +2.0V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V<sub>CC</sub> +1V.
- (5) PE and ORG pin leakage current (I<sub>LI</sub> and I<sub>LO</sub>) = 15 µA max. (at V<sub>IL</sub>), 10 µA otherwise.

INSTRUCTION SET<sup>(6)</sup>

Instruction	Start Bit	Opcode	Address		Data		PE	Comments
			1024 x 8	512 x 16	1024 x 8	512 x 16		
READ	1	1 0	XA9-A0	XA8-A0			X	Start Address AN-A0
ERASE	1	1 1	XA9-A0	XA8-A0			1	Clear Address AN-A0
WRITE	1	0 1	XA9-A0	XA8-A0	D7-D0	D15-D0	1	Write Address AN-A0
EWEN	1	0 0	11XXXXXXXXXX	11XXXXXXXXXX			X	Write Enable
EWDS	1	0 0	00XXXXXXXXXX	00XXXXXXXXXX			X	Write Disable
ERAL	1	0 0	10XXXXXXXXXX	10XXXXXXXXXX			1	Clear All Addresses
WRAL	1	0 0	01XXXXXXXXXX	01XXXXXXXXXX	D7-D0	D15-D0	1	Write All Addresses

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## A.C. CHARACTERISTICS

CAT33C108 T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = +3V±10%, unless otherwise specified.CAT33C108I T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = +3V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t <sub>CS</sub>	CS Setup Time	250			ns	
t <sub>CSH</sub>	CS Hold Time	0			ns	
t <sub>DIS</sub>	DI Setup Time	250			ns	C <sub>L</sub> = 100pF V <sub>OL</sub> = 0.3V, V <sub>OH</sub> = V <sub>CC</sub> - 0.3 V <sub>IL</sub> = 0.3V, V <sub>IH</sub> = V <sub>CC</sub> - 0.3
t <sub>DIH</sub>	DI Hold Time	250			ns	
t <sub>PD1</sub>	Output Delay to 1			500	ns	
t <sub>PD0</sub>	Output Delay to 0			500	ns	
t <sub>HZ</sub> <sup>(3)</sup>	Output Delay to High-Z			500	ns	
t <sub>EW</sub> <sup>(7)</sup>	Program/Erase Pulse Width			5	ms	
t <sub>CSMIN</sub>	Minimum CS Low Time	500			ns	
t <sub>SKHI</sub>	Minimum SK High Time	500			ns	
t <sub>SKLOW</sub>	Minimum SK Low time	500			ns	
t <sub>SV</sub>	Output Delay to Status Valid			500	ns	C <sub>L</sub> = 100pF
SK <sub>MAX</sub>	Maximum Clock Frequency	DC		1	MHZ	

Note:

(3) This parameter is tested initially and after a design or process change that affects the parameter.

(6) X indicates a "Don't Care" input (either 0 or 1).

(7) ERAL and WRAL instructions = 10 ms max.

**DEVICE OPERATION**

The CAT33C108/CAT33C108I is a 8192 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT33C108/CAT33C108I can be organized as either 512 registers by 16 bits, or as 1024 registers by 8 bits. Seven 13 bit instructions (14 bit instruction in 1024 by 8 organization) control the reading, writing and erase operations of the device. The CAT33C108/CAT33C108I operates on a single 3V supply and will generate on chip, the high voltage required during any write operation.

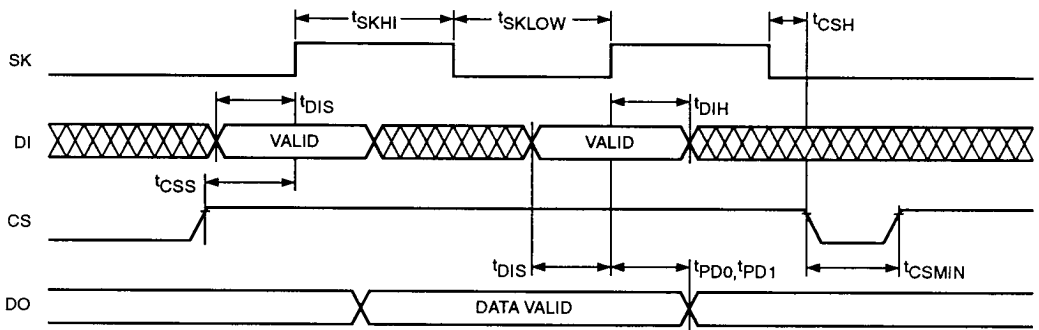
Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling

the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common D/I/O pin.

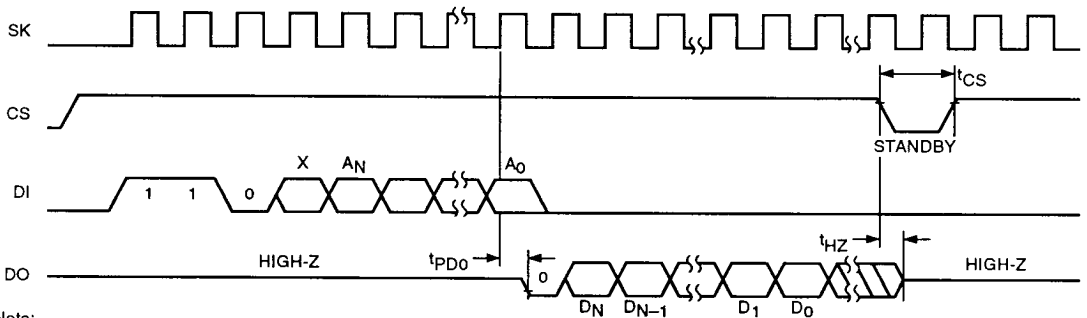
The format for all instructions sent to the CAT33C108/CAT33C108I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 9 bit address (10 bit address when organized as 1024 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 1024 x 8). All program/erase cycles are enabled only when pin 7 (PE) is held high.

**Figure 1. Synchronous Data Timing (8)**



5052 FHD F03

**Figure 2. Read Instruction Timing (8)(9)**



5052 FHD F04

Note:

(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A9 and DN = D7.

When x16 organization is selected, AN = A8 and DN = D15.

(9) PE = "Don't Care".

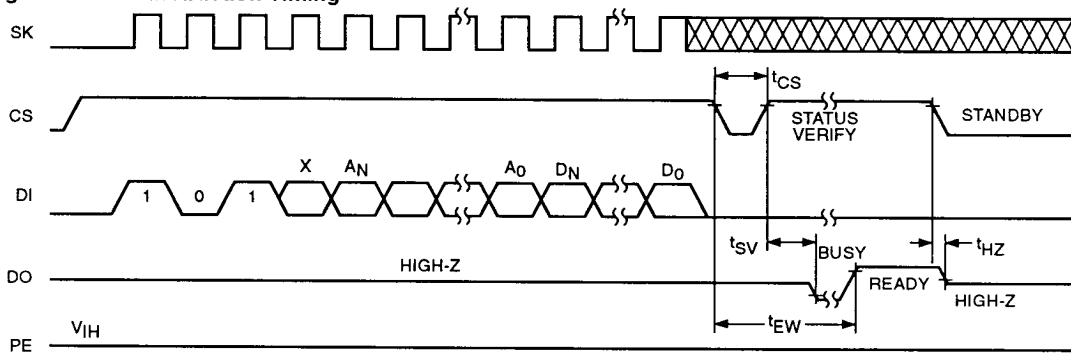
**Read**

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT33C108/CAT33C108I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ( $t_{PD0}$  or  $t_{PD1}$ ). The data output is sequential with the data from address N followed by the data from address N+1. The data output continues to the highest address and will wrap around to the first address if the clock continues to run. Bringing CS low at any time will stop the data output. The dummy bit is suppressed in the sequential read mode (except for the very first address) and a continuous stream of data results.

**Write**

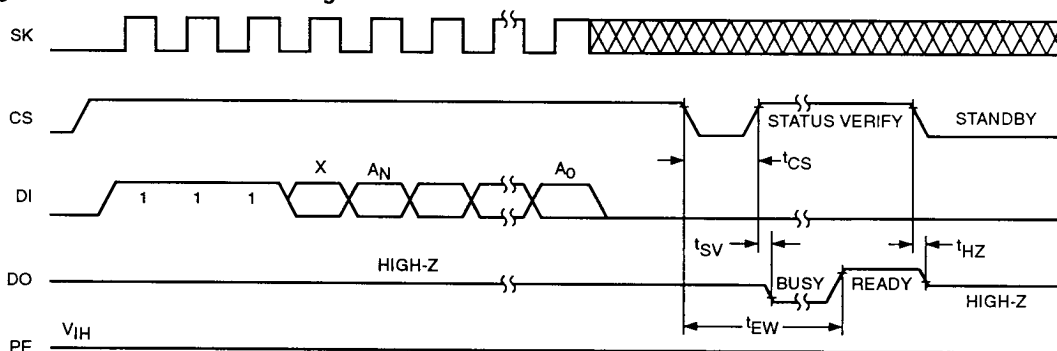
After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 500ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C108/CAT33C108I can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent. The Write instruction requires that PE = 1.

**Figure 3. Write Instruction Timing (8)**



5052 FHD F05

**Figure 4. Erase Instruction Timing (8)**



5052 FHD F07

Note:  
 (8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A9 and DN = D7. When x16 organization is selected, AN = A8 and DN = D15.

**Erase**

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 500ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C108/CAT33C108I can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state. The Erase instruction requires that PE = 1.

**Erase/Write Enable and Disable**

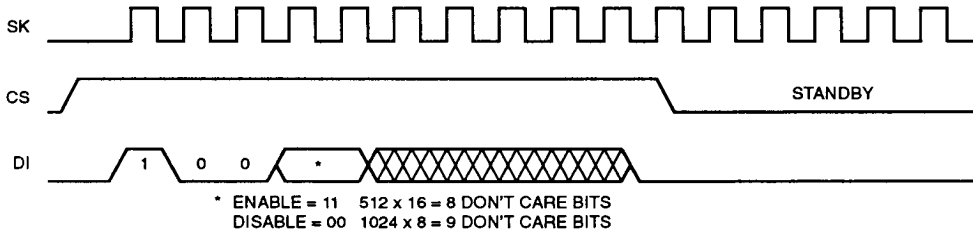
The CAT33C108/CAT33C108I powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power

to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT33C108/CAT33C108I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

**Erase All**

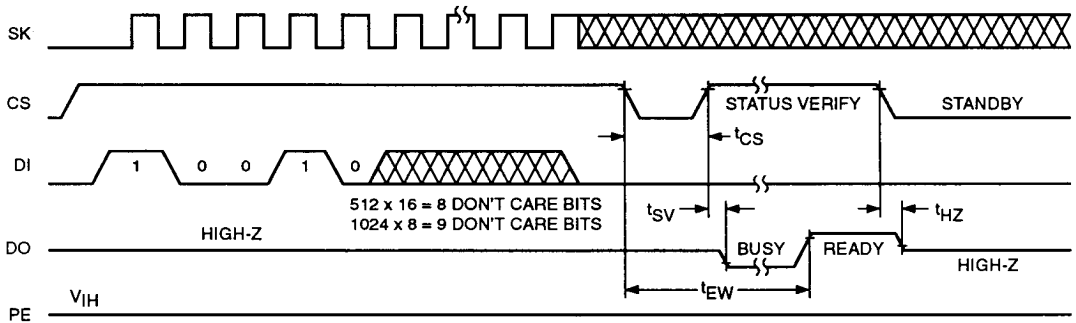
Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 500ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C108/CAT33C108I can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state. The Erase All instruction requires that PE = 1.

**Figure 5. EWEN/EWDS Instruction Timing (8)(9)**



5052 FHD F06

**Figure 6. ERAL Instruction Timing (8)**



5052 FHD F06

Note:

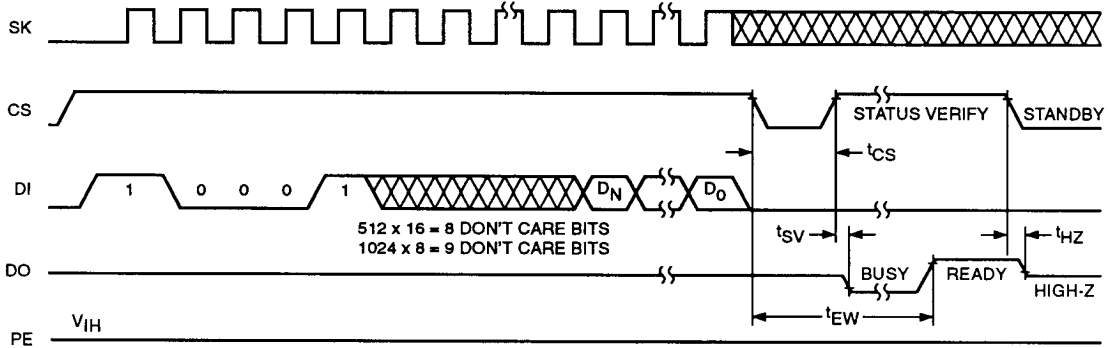
- (8) The ORG pin is used to configure the device for x8 or x16 operation.
- (9) PE = "Don't Care".

**Write All**

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 500ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the

device has entered the self clocking mode. The ready/busy status of the CAT33C108/CAT33C108I can be determined by selecting the device and polling the DO pin. It IS NOT necessary for all memory locations to be cleared before the WRAL command is executed. The Write All instruction requires that PE = 1.

**Figure 7. WRAL Instruction Timing (8)**



**Note:**

(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, DN = D7. When x16 organization is selected, DN = D15.

5052 FHD F09

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