

# CAT32C101

## 1K-Bit SERIAL E<sup>2</sup>PROM

### FEATURES

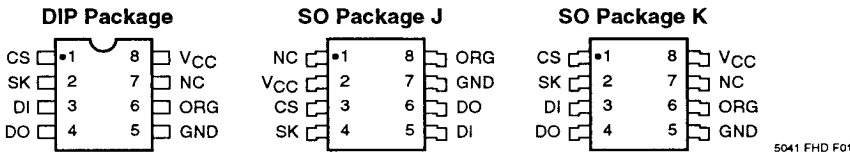
- Low Power CMOS Technology
- 2.2 to 3.5V Operation
- 64 x 16 or 128 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- 1.9V Read Operation
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

### DESCRIPTION

The CAT32C101 is a 1K bit Serial E<sup>2</sup>PROM memory device which can be configured as either 64 registers by 16 bits (ORG pin at V<sub>CC</sub>) or 128 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT32C101 is

manufactured using Catalyst's advanced CMOS E<sup>2</sup>PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

### PIN CONFIGURATION

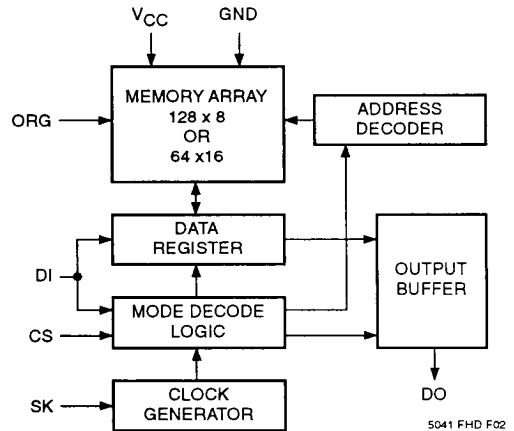


### PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V <sub>CC</sub>	+2.2V to +3.5V Power Supply
GND	Ground
NC	No Connection
ORG	Memory Organization

Note: When the ORG pin is connected to V<sub>CC</sub>, the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64 x 16 organization.

### BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with Respect to Ground <sup>(1)</sup> .....	-2.0V to +V <sub>CC</sub> +2.0V
V <sub>CC</sub> with Respect to Ground .....	-2.0V to +7.0V
Package Power Dissipation Capability (T <sub>a</sub> = 25°C) .....	1.0W
Lead Soldering Temperature (10 secs) .....	300°C
Output Short Circuit Current <sup>(2)</sup> .....	100 mA

**\*COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

**RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N <sub>END</sub> <sup>(3)</sup>	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T <sub>DR</sub> <sup>(3)</sup>	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V <sub>ZAP</sub> <sup>(3)</sup>	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I <sub>LTH</sub> <sup>(3)(4)</sup>	Latch-Up	100		mA	JEDEC Standard 17

**D.C. OPERATING CHARACTERISTICS**

CAT32C101 T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = +2.2V to +3.5V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I <sub>CC1</sub>	Power Supply Current (Operating)			2	mA	DI = 0.0V, SK = 3.5V V <sub>CC</sub> = 3.5V, CS = 3.5V, Output Open
I <sub>CC2</sub>	Power Supply Current (Standby)			2	μA	V <sub>CC</sub> = 3.5V, CS = 0V DI = 0V SK = 0V ORG = 3.5V
I <sub>LI</sub>	Input Leakage Current			2	μA	V <sub>IN</sub> = 0V to 3.5V
I <sub>LO</sub>	Output Leakage Current (Including ORG Pin)			10	μA	V <sub>OUT</sub> = 0V to 3.5V, CS = 0V
V <sub>IH</sub>	High Level Input Voltage	V <sub>CC</sub> - 0.3		V <sub>CC</sub> + 1	V	
V <sub>IL</sub>	Low Level Input Voltage	-0.1		0.3	V	
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> - 0.3			V	I <sub>OH</sub> = -10μA
V <sub>OL</sub>	Low Level Output Voltage			0.3	V	I <sub>OL</sub> = 10μA

## Note:

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> +0.5V, which may overshoot to V<sub>CC</sub> +2.0V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V<sub>CC</sub> +1V.

## INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1 0	A6-A0	A5-A0			Read Address AN-A0
ERASE	1	1 1	A6-A0	A5-A0			Clear Address AN-A0
WRITE	1	0 1	A6-A0	A5-A0	D7-D0	D15-D0	Write Address AN-A0
EWEN	1	0 0	11XXXXX	11XXXX			Write Enable
EWDS	1	0 0	00XXXXX	00XXXX			Write Disable
ERAL	1	0 0	10XXXXX	10XXXX			Clear All Addresses
WRAL	1	0 0	01XXXXX	01XXXX	D7-D0	D15-D0	Write All Addresses

3

## A.C. CHARACTERISTICS

CAT32C101  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +2.2\text{V}$  to  $+3.5\text{V}$ , unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t <sub>CS</sub>	CS Setup Time	200			ns	
t <sub>CSH</sub>	CS Hold Time	0			ns	$C_L = 100\text{pF}$
t <sub>DIS</sub>	DI Setup Time	400			ns	$V_{OL} = 0.3\text{V}$
t <sub>DIH</sub>	DI Hold Time	400			ns	$V_{OH} = V_{CC} - 0.3$
t <sub>PD1</sub>	Output Delay to 1			2	$\mu\text{s}$	$V_{IL} = 0.3\text{V}$
t <sub>PD0</sub>	Output Delay to 0			2	$\mu\text{s}$	$V_{IH} = V_{CC} - 0.3$
t <sub>HZ</sub> <sup>(3)</sup>	Output Delay to High-Z			400	ns	
t <sub>EW</sub>	Program/Erase Pulse Width			20	ms	
t <sub>CSMIN</sub>	Minimum CS Low Time	1			$\mu\text{s}$	
t <sub>SKHI</sub>	Minimum SK High Time	1			$\mu\text{s}$	
t <sub>SKLOW</sub>	Minimum SK Low time	1			$\mu\text{s}$	
t <sub>SV</sub>	Output Delay to Status Valid			1	$\mu\text{s}$	$C_L = 100\text{pF}$
SK <sub>MAX</sub>	Maximum Clock Frequency	DC		250	kHz	

Note:

(3) This parameter is tested initially and after a design or process change that affects the parameter.

## DEVICE OPERATION

The CAT32C101 is a 1024 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT32C101 can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Seven 9 bit instructions (10 bit instruction in 128 by 8 organization) control the reading, writing and erase operations of the device. The CAT32C101 operates on a single 2.2–3.5V supply and will generate on chip, the high voltage required during any write operation.

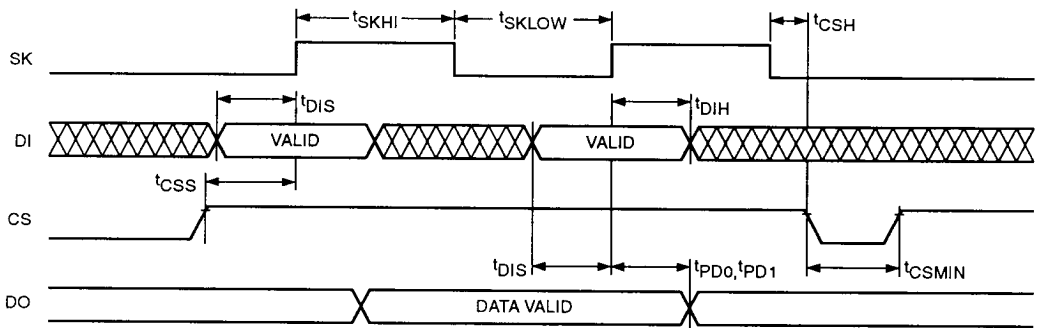
Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write

operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

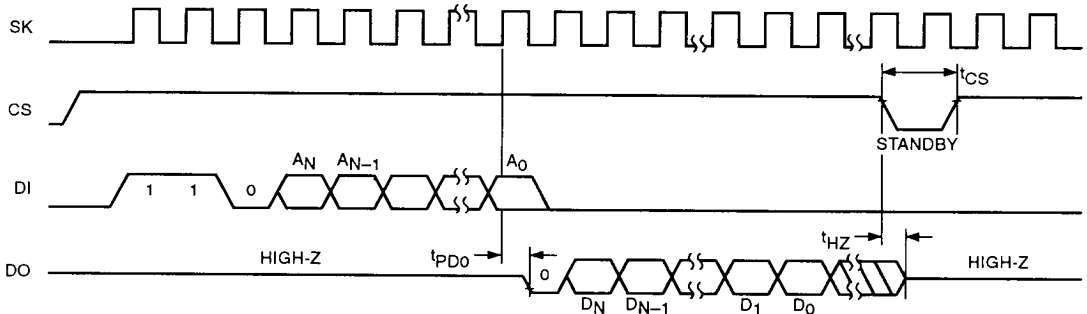
The format for all instructions sent to the CAT32C101 is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 6 bit address (7 bit address when organized as 128 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 x 8).

Figure 1. Synchronous Data Timing (5)



5041 FHD F03

Figure 2. Read Instruction Timing (5)



5041 FHD F04

Note:

- (5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

At power-down, when  $V_{CC}$  falls below a threshold of approximately 1.7V, the data protection circuitry inhibits the erase and write instructions and a write disable (EWDS) is executed internally.

NOTE: This device will accept a start bit that is generated when both SK and DI are high with respect to a low to high transition of CS.

**Read**

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT32C101 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ( $t_{PD0}$  or  $t_{PD1}$ ).

**Write**

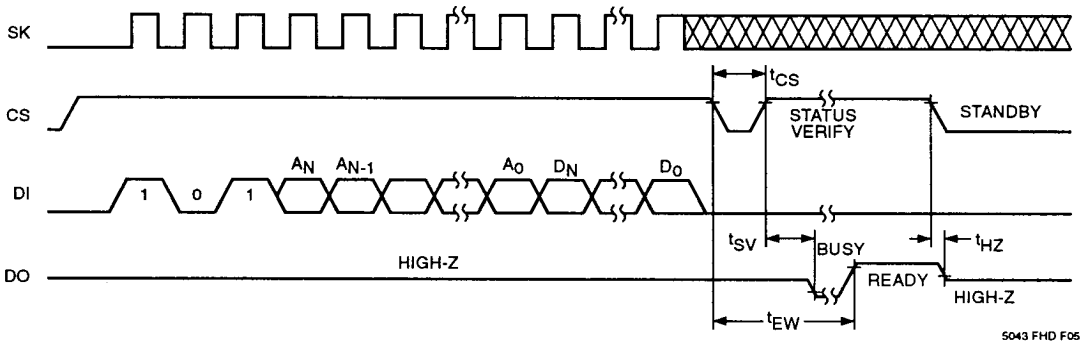
After receiving a WRITE command, address and the

data, the CS (chip select) pin must be deselected for a minimum of  $1\mu s$  ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT32C101 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

**Erase**

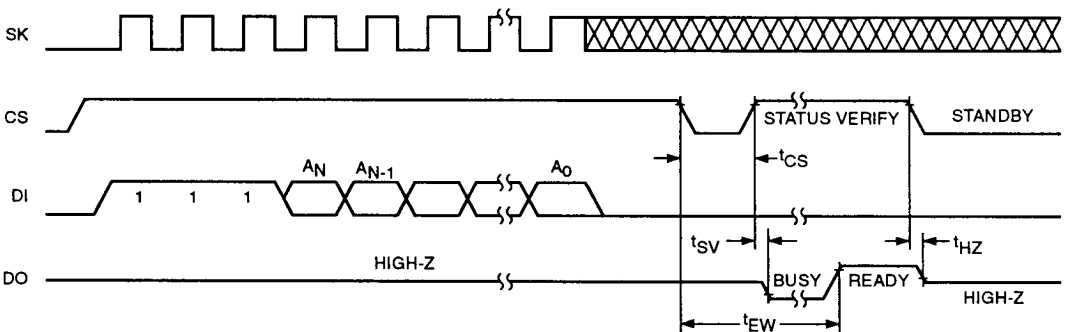
Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of  $1\mu s$  ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT32C101 can be determined by selecting the device and polling the DO pin.

Figure 3. Write Instruction Timing (5)



5043 FHD F05

Figure 4. Erase Instruction Timing (5)



5041 FHD F07

Note:

- (5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

Once cleared, the content of a cleared location returns to a logical "1" state.

**Erase/Write Enable and Disable**

The CAT32C101 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT32C101 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

**Erase All**

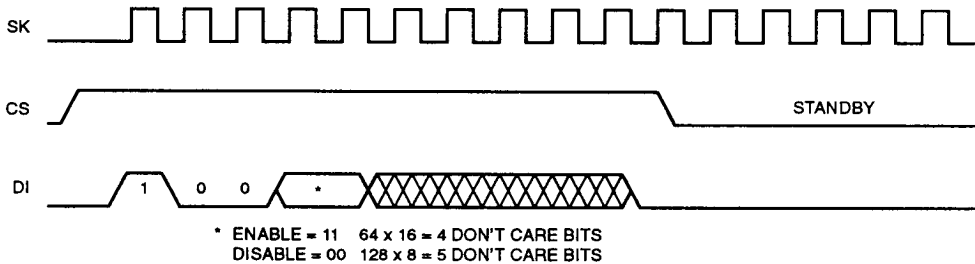
Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 1µs (tCSMIN).

The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT32C101 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

**Write All**

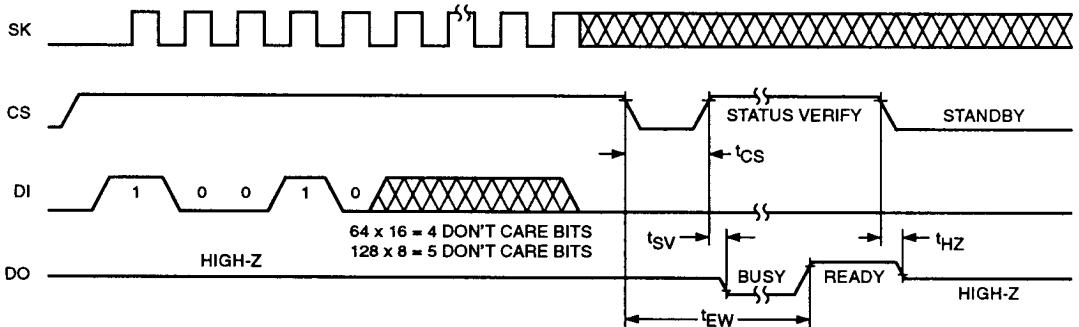
Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 1µs (tCSMIN). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT32C101 can be determined by selecting the device and polling the DO pin. It is necessary for all memory locations to be cleared before the WRAL command is executed.

**Figure 5. EWEN/EWDS Instruction Timing (5)**



5041 FHD F06

**Figure 6. ERAL Instruction Timing (5)**



5041 FHD F08

**Note:**

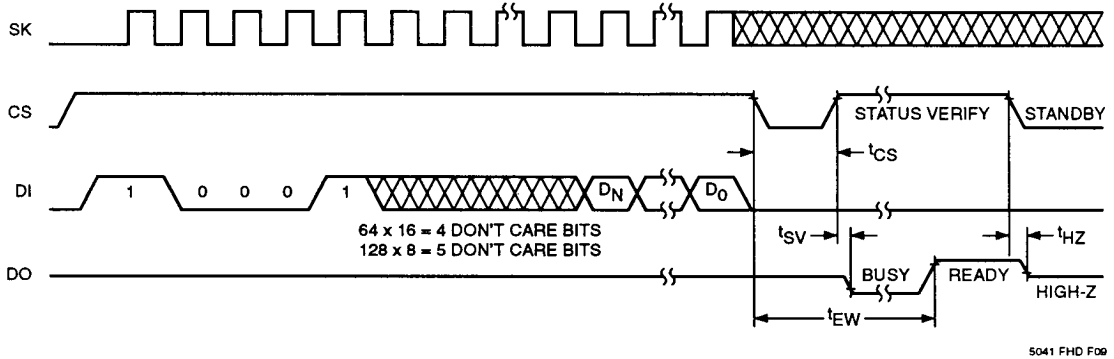
- (5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

**Start Bit Timing**

The CAT32C101 features an alternate start bit timing where the device will accept a start bit that is generated when both SK and DI are high with respect to a low to high transition of CS (see Figure 8). This allows the user to

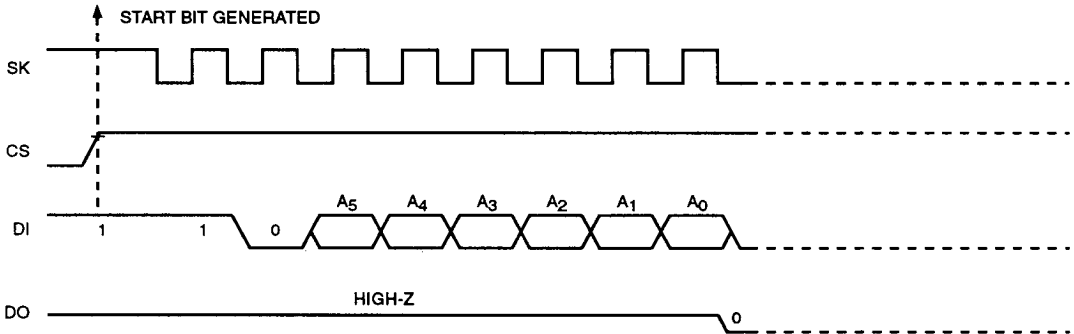
send instructions from microprocessors that transmit and receive data using a sequence of 8 clock cycles only. Once this start bit is generated all subsequent data is clocked into the device on the positive clock edge of SK.

**Figure 7. WRAL Instruction Timing (5)**



5041 FHD F09

**Figure 8. Alternate Start Bit Timing Example: Read Instruction (x 16) (5)**



5041 FHD F10

**Note:**

- (5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected,  $A_N = A_6$  and  $D_N = D_7$ . When x16 organization is selected,  $A_N = A_5$  and  $D_N = D_{15}$ .