

LOW VOLTAGE PARALLEL ACCESS 64K (8K x 8) EEPROM

PRELIMINARY DATA

- FAST ACCESS TIME: 150ns
- SINGLE 3.3V ± 10% SUPPLY VOLTAGE
- LOW POWER CONSUMPTION
- FAST WRITE CYCLE
 - 32 Bytes Page Write Operation
 - Byte or Page Write Cycle: 10ms
- ENHANCED END OF WRITE DETECTION
 - Ready/Busy Open Drain Output (for M28LV64C product only)
 - Data Polling
 - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABILITY SINGLE POLYSILICON, CMOS TECHNOLOGY
 - Endurance > 100,000 Erase/Write Cycles
 - Data Retention > 10 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- ADDRESS and DATA LATCHED ON-CHIP

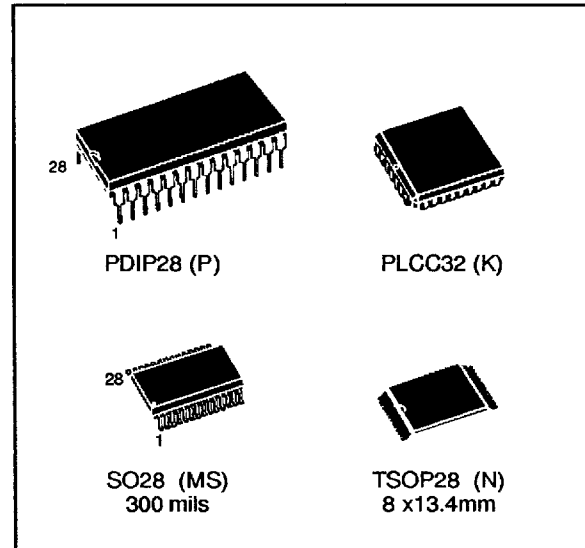


Figure 1. Logic Diagram

DESCRIPTION

The M28LV64C is an 8K x 8 low power EEPROM fabricated with SGS-THOMSON proprietary single polysilicon CMOS technology. The device offers fast access time with low power dissipation and requires a 3.3V power supply.

Table 1. Signal Names

A0 - A12	Address Input
DQ0 - DQ7	Data Input / Output
\overline{W}	Write Enable
\overline{E}	Chip Enable
\overline{G}	Output Enable
\overline{RB}	Ready / Busy
V _{CC}	Supply Voltage
V _{SS}	Ground

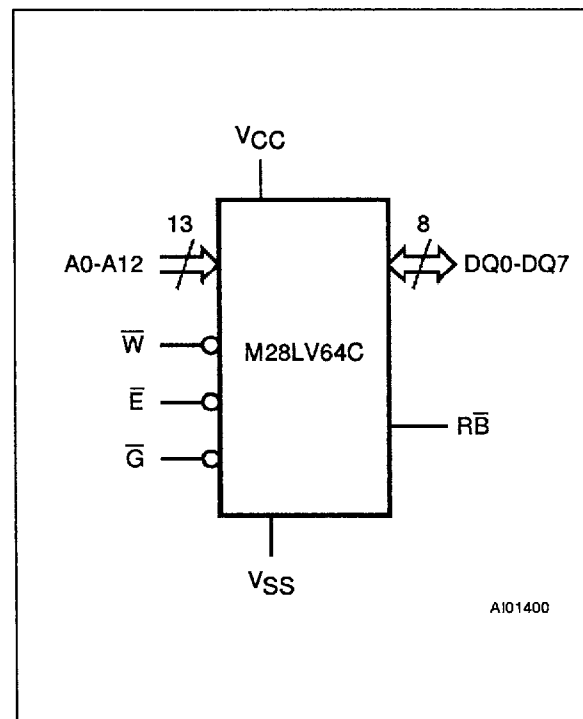


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature: grade 1 grade 6	0 to 70 - 40 to 85	°C
T _{STG}	Storage Temperature Range	- 65 to 150	°C
V _{CC}	Supply Voltage	- 0.3 to 6.5	V
V _{IO}	Input/Output Voltage	- 0.3 to V _{CC} +0.6	V
V _I	Input Voltage	- 0.3 to 6.5	V
V _{ESD}	Electrostatic Discharge Voltage (Human Body model)	2000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2A. DIP Pin Connections

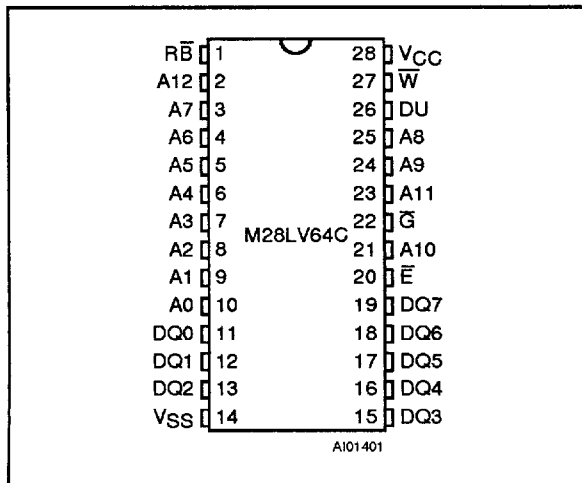


Figure 2B. LCC Pin Connections

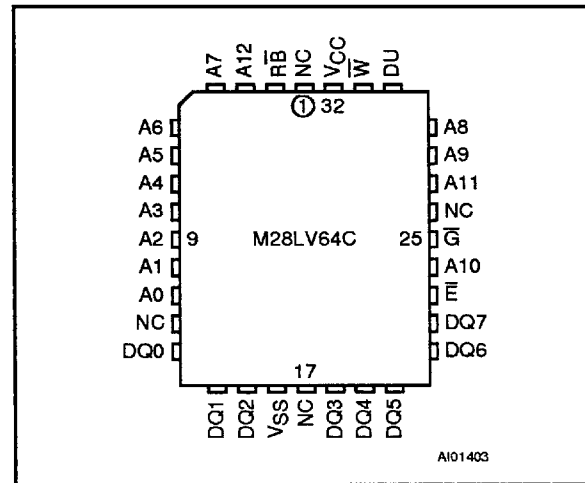


Figure 2C. SO Pin Connections

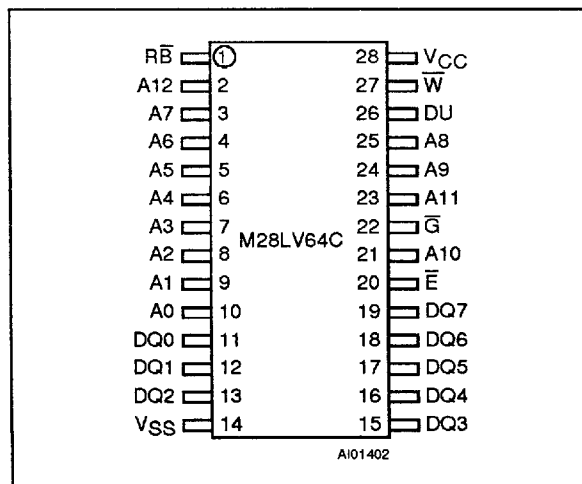


Figure 2D. TSOP Pin Connections

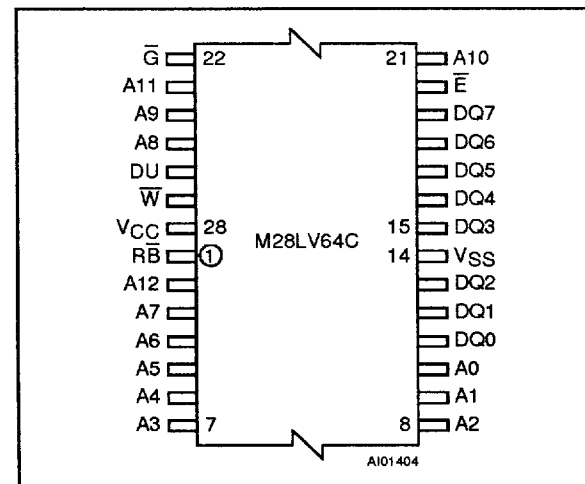


Figure 3. Block Diagram

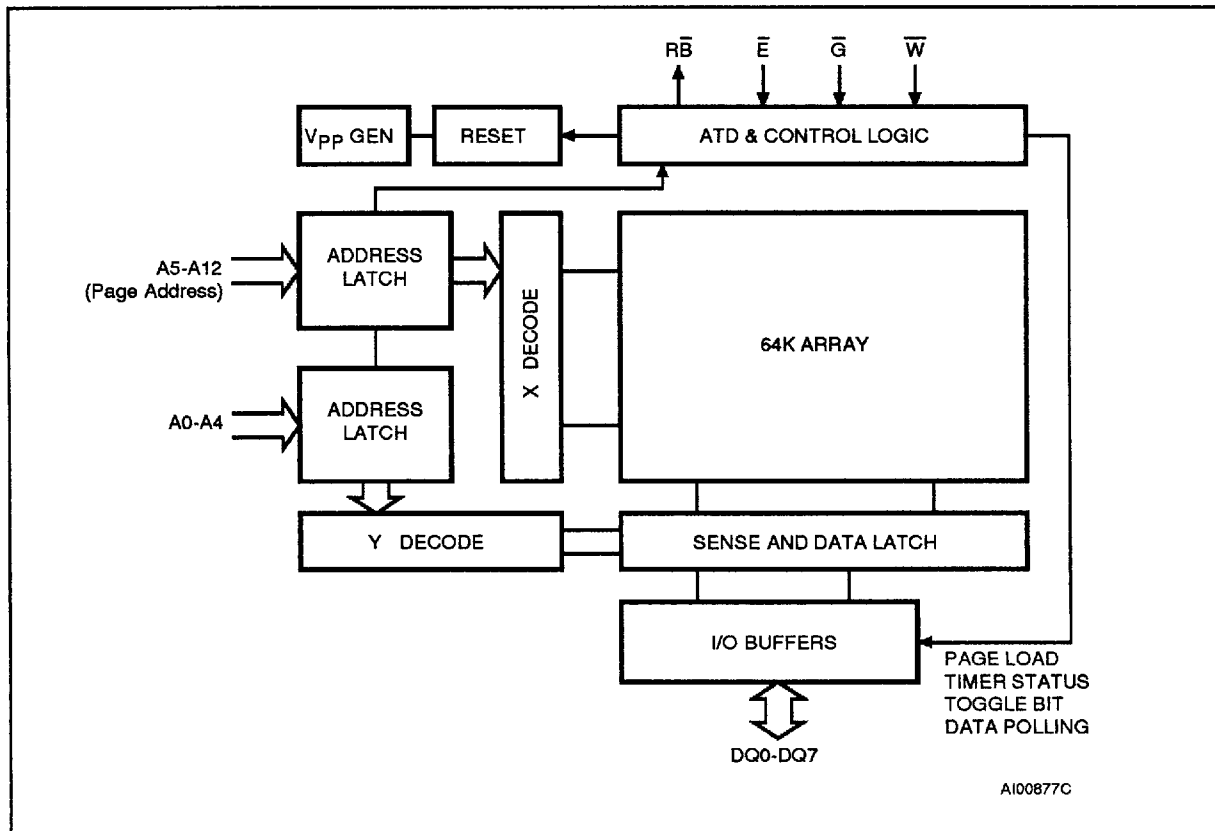


Table 3. Operating Modes

Mode	\bar{E}	\bar{G}	\bar{W}	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z

Note: X = V_{IH} or V_{IL}

DESCRIPTION (cont'd)

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking mode with Ready/Busy, Data Polling and Toggle Bit. The M28LV64C supports 32 byte page write operation.

PIN DESCRIPTION

Addresses (A0-A12). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (\bar{E}). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable (\bar{G}). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28LV64C through the I/O pins.

Write Enable (\bar{W}). The Write Enable input controls the writing of data to the M28LV64C.

Ready/Busy (\bar{RB}). Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle.

OPERATION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming circuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 6.

Read

The M28LV64C is accessed like a static RAM. When \bar{E} and \bar{G} are low with \bar{W} high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either \bar{G} or \bar{E} is high.

Write

Write operations are initiated when both \bar{W} and \bar{E} are low and \bar{G} is high. The M28LV64C supports both \bar{E} and \bar{W} controlled write cycles. The Address is latched by the falling edge of \bar{E} or \bar{W} which ever occurs last and the Data on the rising edge of \bar{E} or \bar{W} which ever occurs first. Once initiated the write operation is internally timed until completion.

Page Write

Page write allows up to 32 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A5-A12 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data after the rising edge of \bar{E} or \bar{W} which ever occurs first. If a transition of \bar{E} or \bar{W} is not detected within t_{WHWH} , the internal programming cycle will start.

Microcontroller Control Interface

The M28LV64C provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the \bar{RB} signal on a separate pin.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
 TB = Toggle Bit
 PLTS = Page Load Timer Status

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28LV64C also offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read any address in the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). In the Page Write mode data may be latched by \bar{E} or \bar{W} . Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low. DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

Ready/Busy pin. The \bar{RB} pin provides a signal at its open drain output which is low during the erase/write cycle, but which is released at the completion of the programming cycle.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times $\leq 20\text{ns}$
 Input Pulse Voltages $0\text{V to } V_{CC} - 0.3\text{V}$
 Input and Output Timing Ref. Voltages 1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Input Output Waveforms

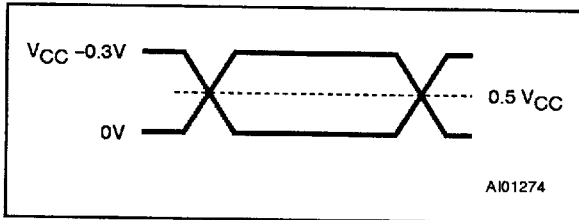


Figure 6. AC Testing Equivalent Load Circuit

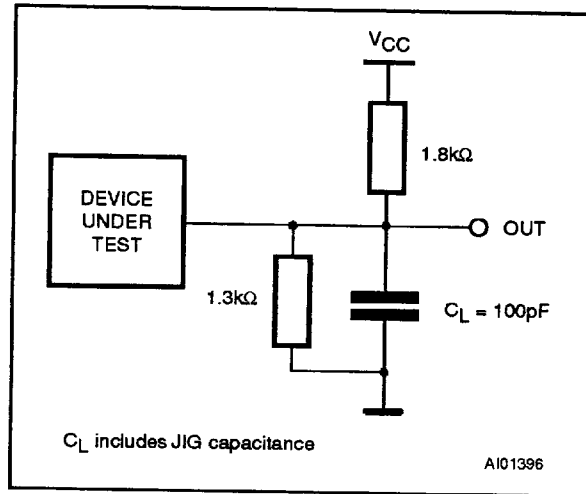


Table 4. Capacitance⁽¹⁾ ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$		6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics ($T_A = 0\text{ to } 70^\circ\text{C}$ or $-40\text{ to } 85^\circ\text{C}$, $V_{CC} = 3\text{V to } 3.6\text{V}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0\text{V} \leq V_{IN} \leq V_{CC}$		1	μA
I_{LO}	Output Leakage Current	$0\text{V} \leq V_{IN} \leq V_{CC}$		10	μA
$I_{CC}^{(1)}$	Supply Current (CMOS inputs)	$\bar{E} = V_{IL}, \bar{G} = V_{IL}, f = 5\text{ MHz}$		15	mA
$I_{CC2}^{(1)}$	Supply Current (Standby) CMOS	$\bar{E} > V_{CC} - 0.3\text{V}$		50	μA
V_{IL}	Input Low Voltage		-0.3	0.6	V
V_{IH}	Input High Voltage		2	$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{ mA}$		0.3	V
V_{OH}	Output High Voltage	$I_{OH} = -1\text{ mA}$	2		V

Note: 1. All I/O's open.

Table 6. Power Up Timing⁽¹⁾ ($T_A = 0\text{ to } 70^\circ\text{C}$ or $-40\text{ to } 85^\circ\text{C}$, $V_{CC} = 3\text{V to } 3.6\text{V}$)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation	1		μs
t_{PUW}	Time Delay to Write Operation	10		ms

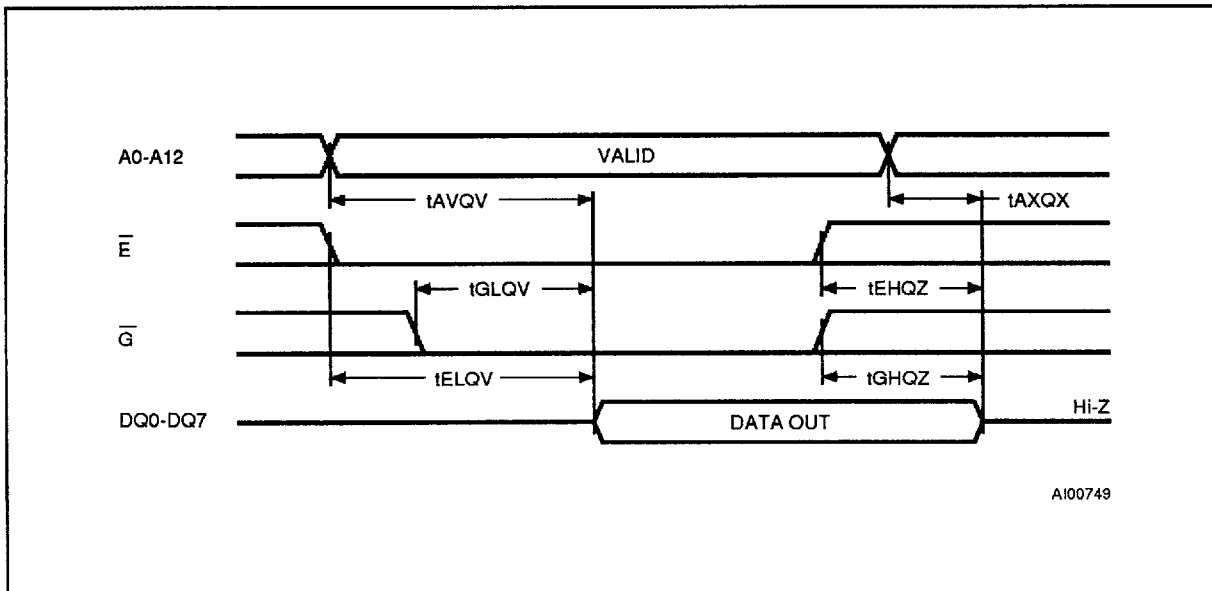
Note: 1. Sampled only, not 100% tested.

Table 7. Read Mode AC Characteristics
 (T_A = 0 to 70°C or -40 to 85°C, V_{CC} = 3V to 3.6V)

Symbol	Alt	Parameter	Test Condition	M28LV64C						Unit
				-150		-200		-300		
				min	max	min	max	min	max	
t _{AVQV}	t _{ACC}	Address Valid to Output Valid	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$		150		200		300	ns
t _{ELQV}	t _{CE}	Chip Enable Low to Output Valid	G = V _{IL}		150		200		300	ns
t _{GLQV}	t _{OE}	Output Enable Low to Output Valid	$\bar{E} = V_{IL}$		75		100		150	ns
t _{EHQZ} ⁽¹⁾	t _{DF}	Chip Enable High to Output Hi-Z	$\bar{G} = V_{IL}$	0	50	0	60	0	60	ns
t _{GHQZ} ⁽¹⁾	t _{DF}	Output Enable High to Output Hi-Z	$\bar{E} = V_{IL}$	0	50	0	60	0	60	ns
t _{AXQX}	t _{OH}	Address Transition to Output Transition	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$	0		0		0		ns

Note: 1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. Read Mode AC Waveforms



Note: \bar{W} = High

Table 8. Write Mode AC Characteristics
 (T_A = 0 to 70°C or -40 to 85°C, V_{CC} = 3V to 3.6V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t _{AVWL}	t _{AS}	Address Valid to Write Enable Low	$\bar{E} = V_{IL}, \bar{G} = V_{IH}$	0		ns
t _{AVEL}	t _{AS}	Address Valid to Chip Enable Low	$\bar{G} = V_{IH}, \bar{W} = V_{IL}$	0		ns
t _{ELWL}	t _{CES}	Chip Enable Low to Write Enable Low	$\bar{G} = V_{IH}$	0		ns
t _{GHWL}	t _{OES}	Output Enable High to Write Enable Low	$\bar{E} = V_{IL}$	0		ns
t _{GHEL}	t _{OES}	Output Enable High to Chip Enable Low	$\bar{W} = V_{IL}$	0		ns
t _{WLLEL}	t _{WES}	Write Enable Low to Chip Enable Low	$\bar{G} = V_{IH}$	0		ns
t _{WLAX}	t _{AH}	Write Enable Low to Address Transition		150		ns
t _{ELAX}	t _{AH}	Chip Enable Low to Address Transition		150		ns
t _{WLDV}	t _{DV}	Write Enable Low to Input Valid	$\bar{E} = V_{IL}, \bar{G} = V_{IH}$		1	μs
t _{ELDV}	t _{DV}	Chip Enable Low to Input Valid	$\bar{G} = V_{IH}, \bar{W} = V_{IL}$		1	μs
t _{WLWH}	t _{WP}	Write Enable Low to Write Enable High		150		ns
t _{LELH}	t _{WP}	Chip Enable Low to Chip Enable High		150		ns
t _{WHEH}	t _{CEH}	Write Enable High to Chip Enable High		0		ns
t _{WHGL}	t _{OEH}	Write Enable High to Output Enable Low		10		ns
t _{EHGL}	t _{OEH}	Chip Enable High to Output Enable Low		10		ns
t _{EHWH}	t _{WEH}	Chip Enable High to Write Enable High		0		ns
t _{WHDX}	t _{DH}	Write Enable High to Input Transition		15		ns
t _{EHDX}	t _{DH}	Chip Enable High to Input Transition		15		ns
t _{WHWL}	t _{WPH}	Write Enable High to Write Enable Low		200		ns
t _{WHWH}	t _{BLC}	Byte Load Repeat Cycle Time		0.35	50	μs
t _{WHRH}	t _{WC}	Write Cycle Time			10	ms
t _{WHRL}	t _{DB}	Write Enable High to Ready/Busy Low	Note 1		150	ns
t _{EHRL}	t _{DB}	Chip Enable High to Ready/Busy Low	Note 1		150	ns
t _{DVWH}	t _{DS}	Data Valid before Write Enable High		50		ns
t _{DVEH}	t _{DS}	Data Valid before Chip Enable High		100		ns

Note: 1. With a 3.3 kΩ pull-up resistor.

Figure 8. Write Mode AC Waveforms - Write Enable Controlled

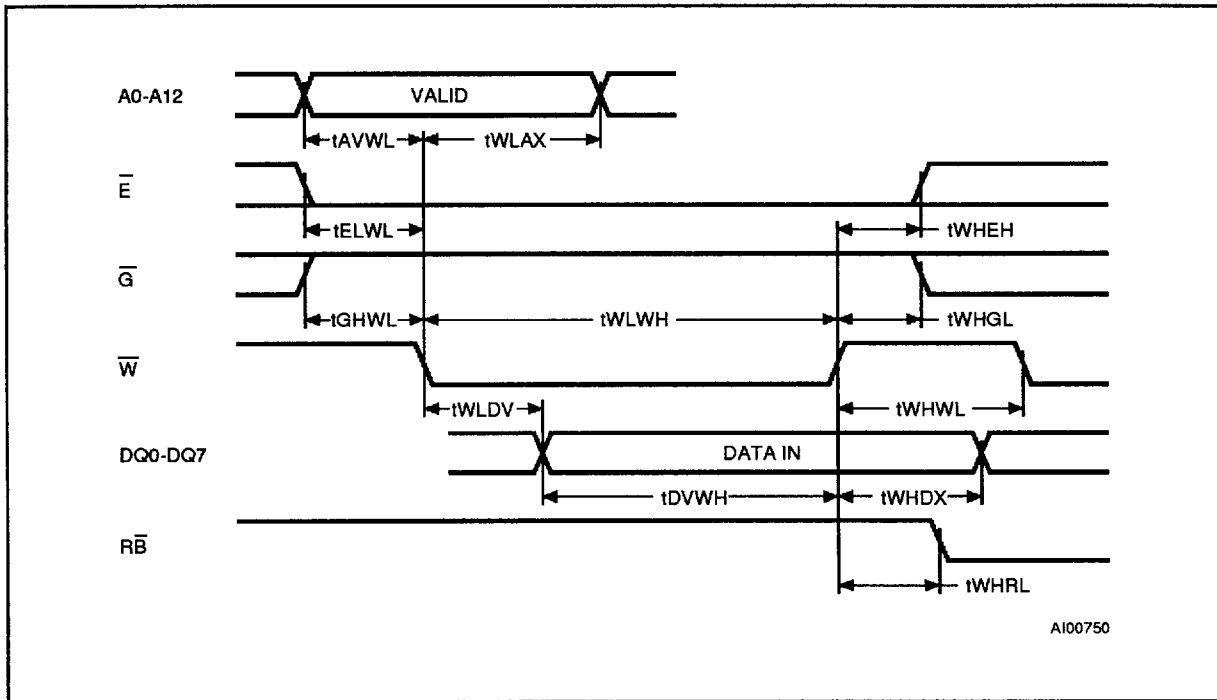


Figure 9. Write Mode AC Waveforms - Chip Enable Controlled

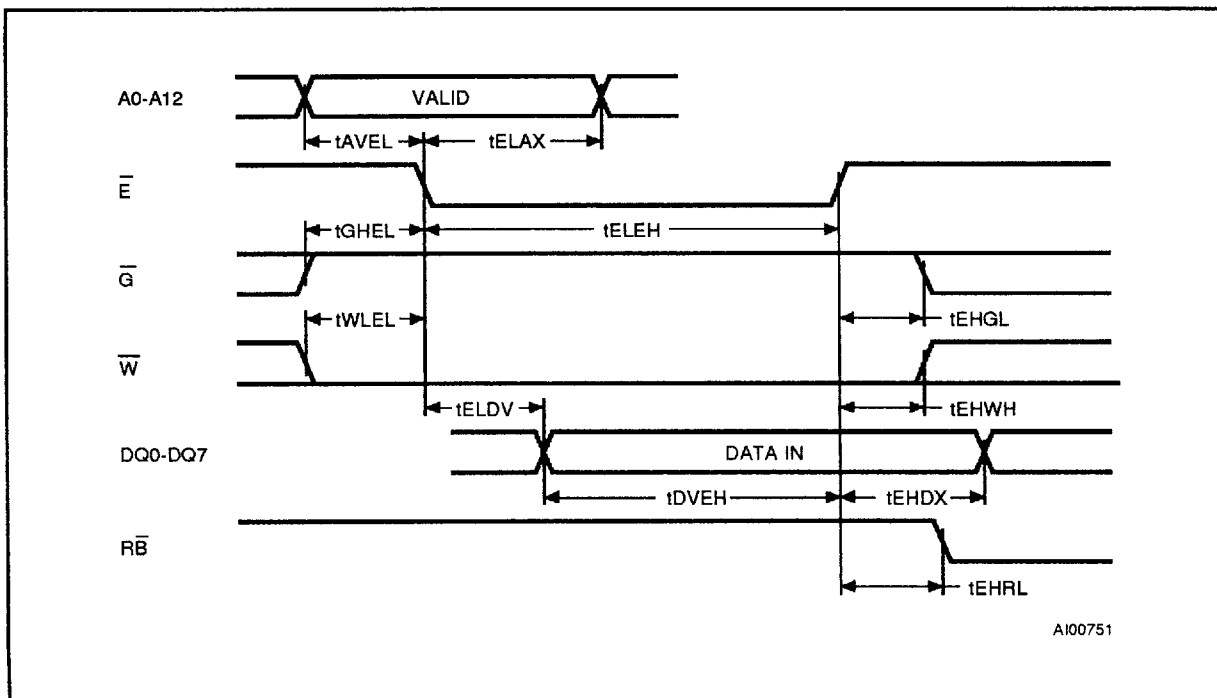


Figure 10. Page Write Mode AC Waveforms - Write Enable Controlled

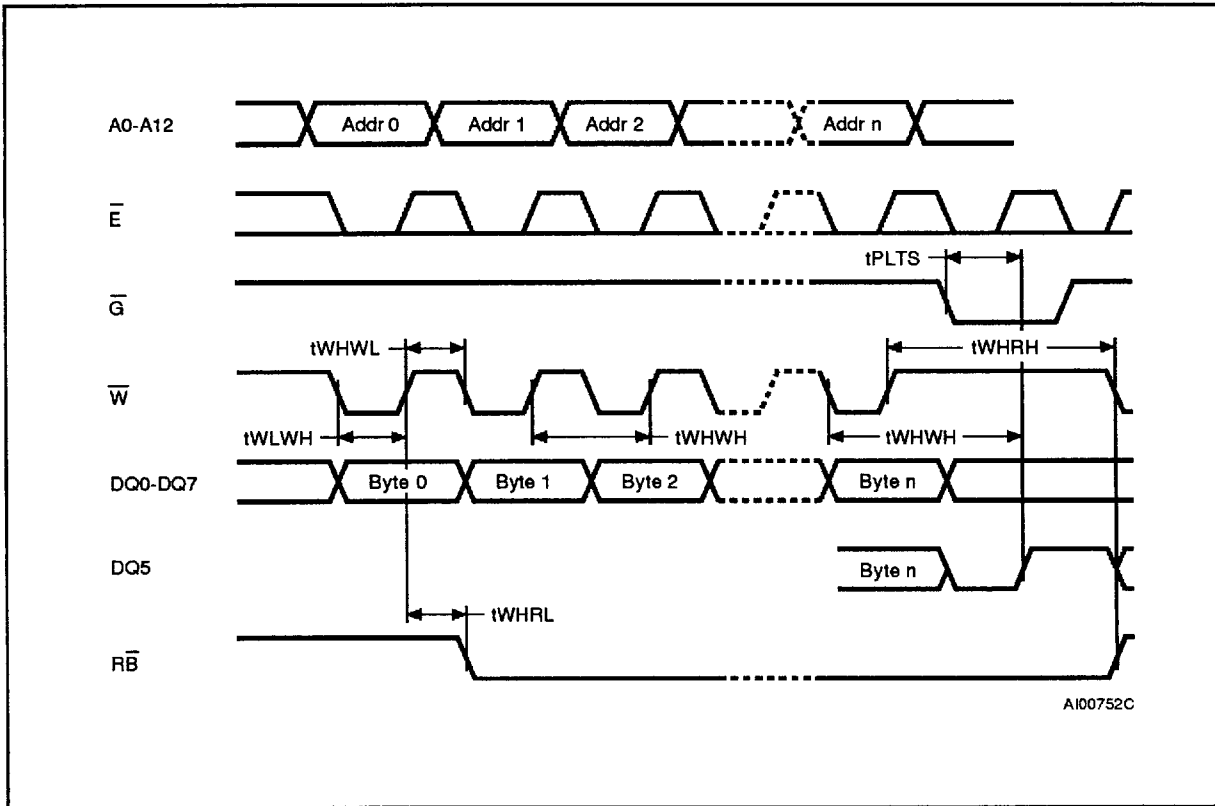


Figure 11. Data Polling Waveforms Sequence

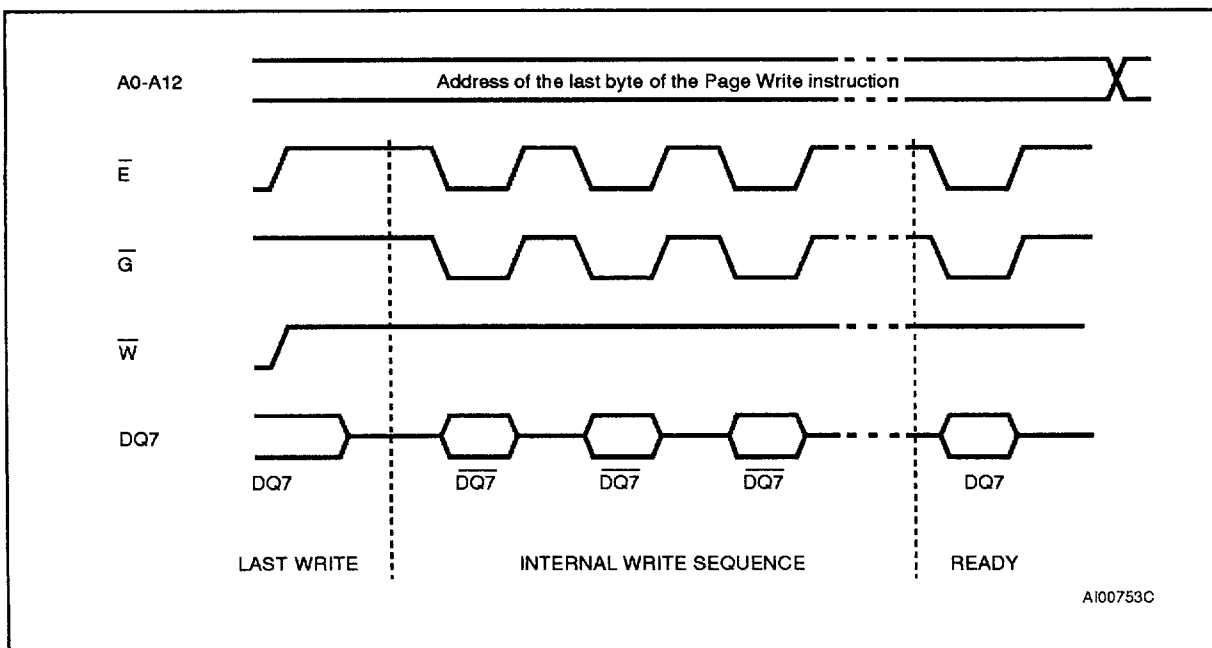
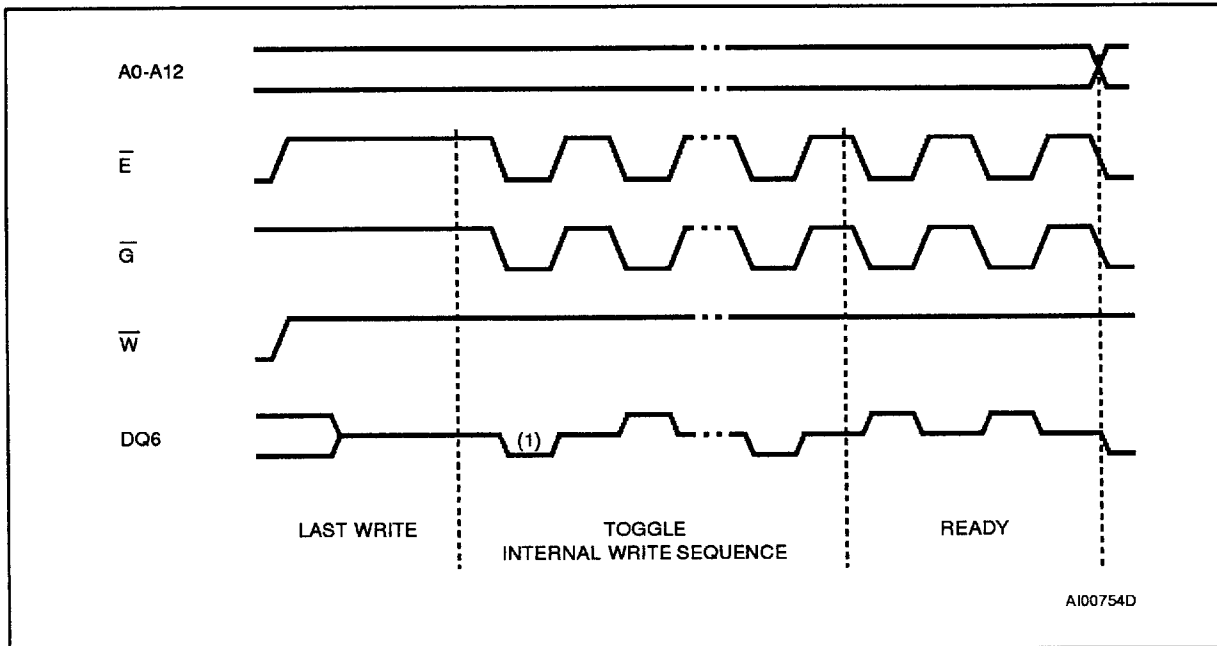
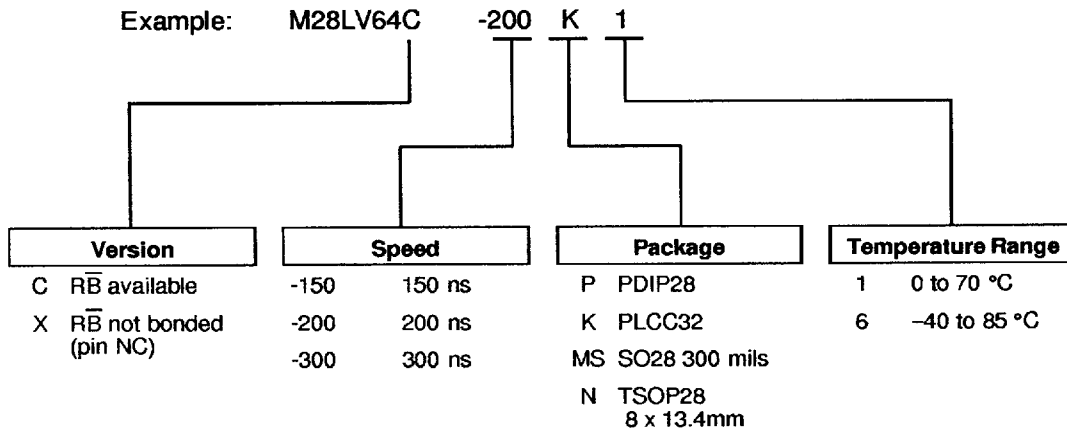


Figure 12. Toggle Bit Waveforms Sequence



Note: 1. First Toggle bit is forced to '0'

ORDERING INFORMATION SCHEME



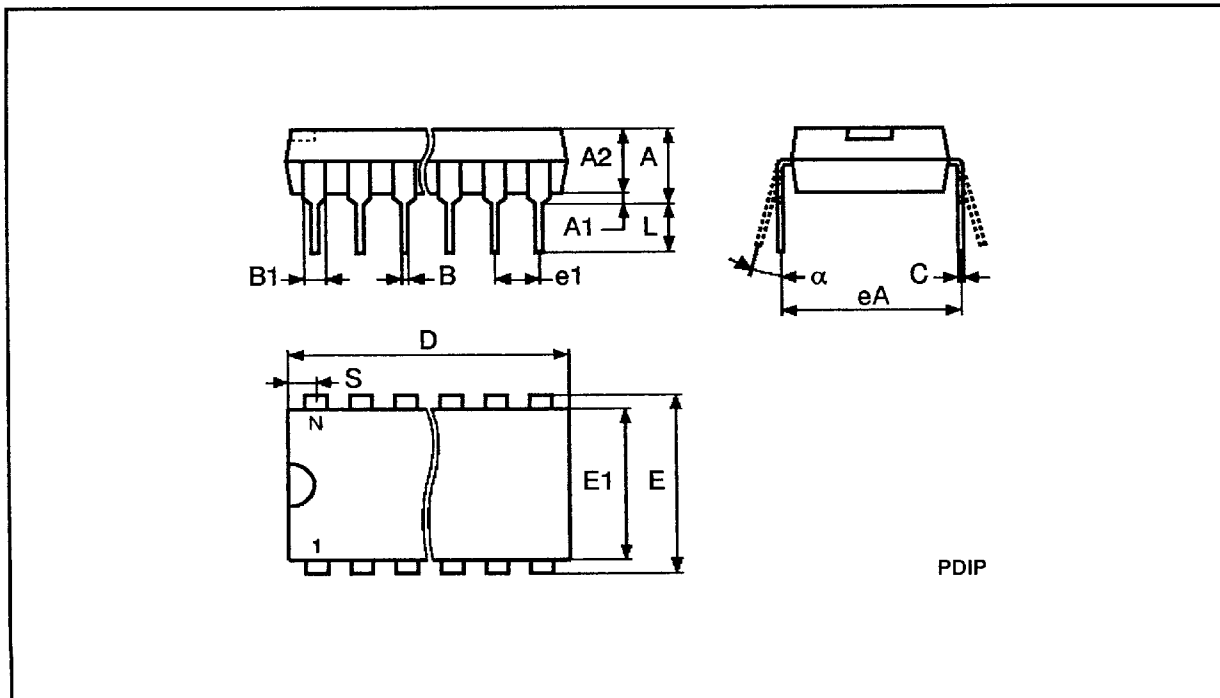
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches			
	Typ	Min	Max	Typ	Min	Max	
A		3.94	5.08		0.155	0.200	
A1		0.38	1.78		0.015	0.070	
A2		3.56	4.06		0.140	0.160	
B		0.38	0.56		0.015	0.021	
B1		1.14	1.78		0.045	0.070	
C		0.20	0.30		0.008	0.012	
D		34.70	37.34		1.366	1.470	
E		14.80	16.26		0.583	0.640	
E1		12.50	13.97		0.492	0.550	
e1	2.54	-	-	0.100	-	-	
eA		15.20	17.78		0.598	0.700	
L		3.05	3.82		0.120	0.150	
S		1.02	2.29		0.040	0.090	
α		0°	15°		0°	15°	
N		28			28		

PDIP28

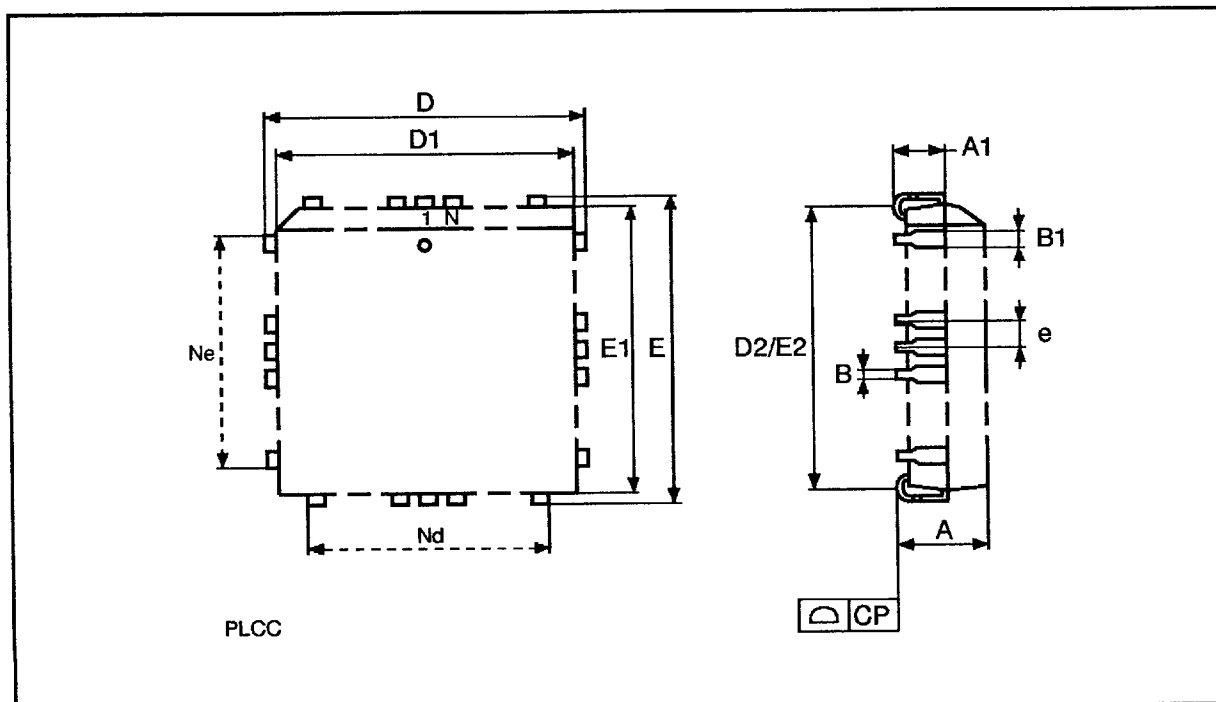


Drawing is not to scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	-	-	0.050	-	-
N		32			32	
Nd		7			7	
Ne		9			9	
CP			0.10			0.004

PLCC32

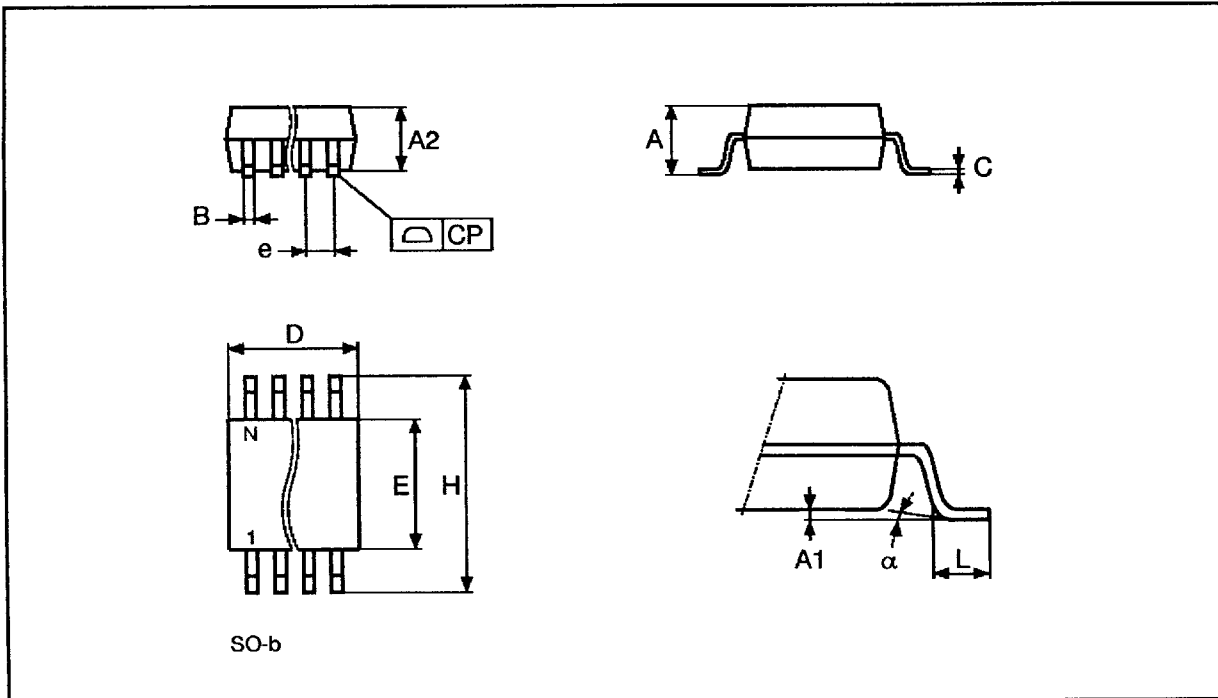


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SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	-	-	0.050	-	-
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N		28			28	
CP			0.10			0.004

SO28

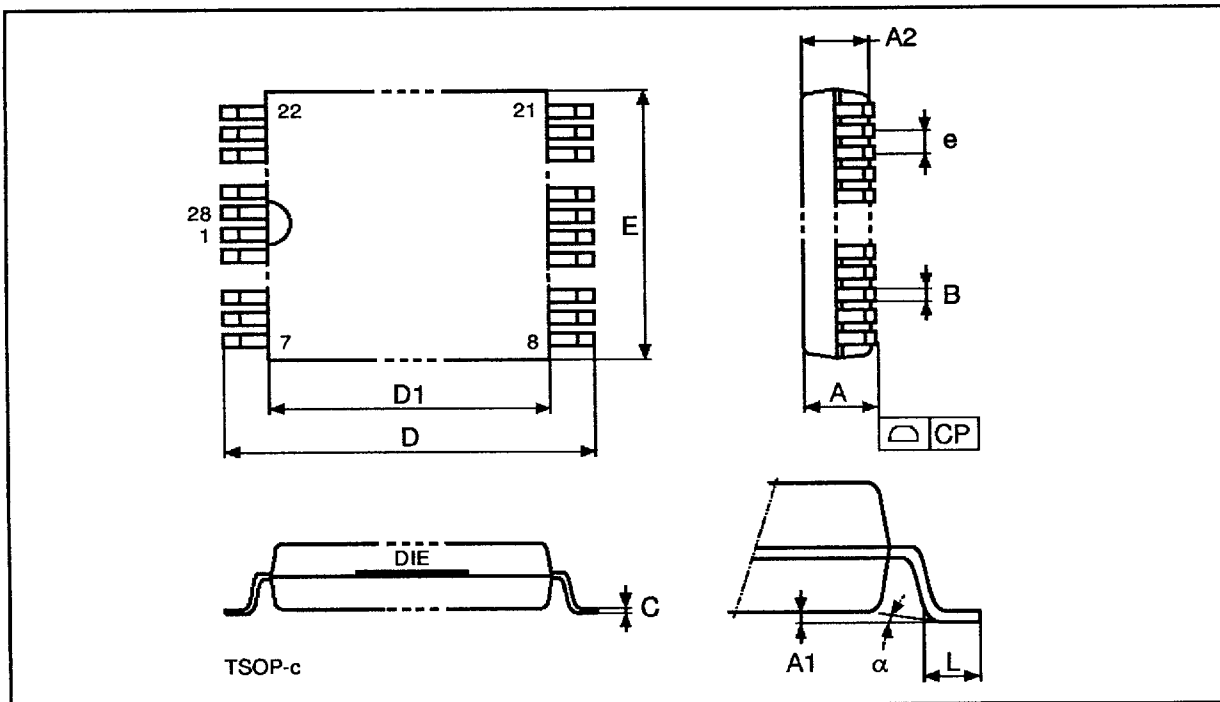


Drawing is not to scale

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	-	-	0.022	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	28			28		
CP			0.10			0.004

TSOP28



Drawing is not to scale