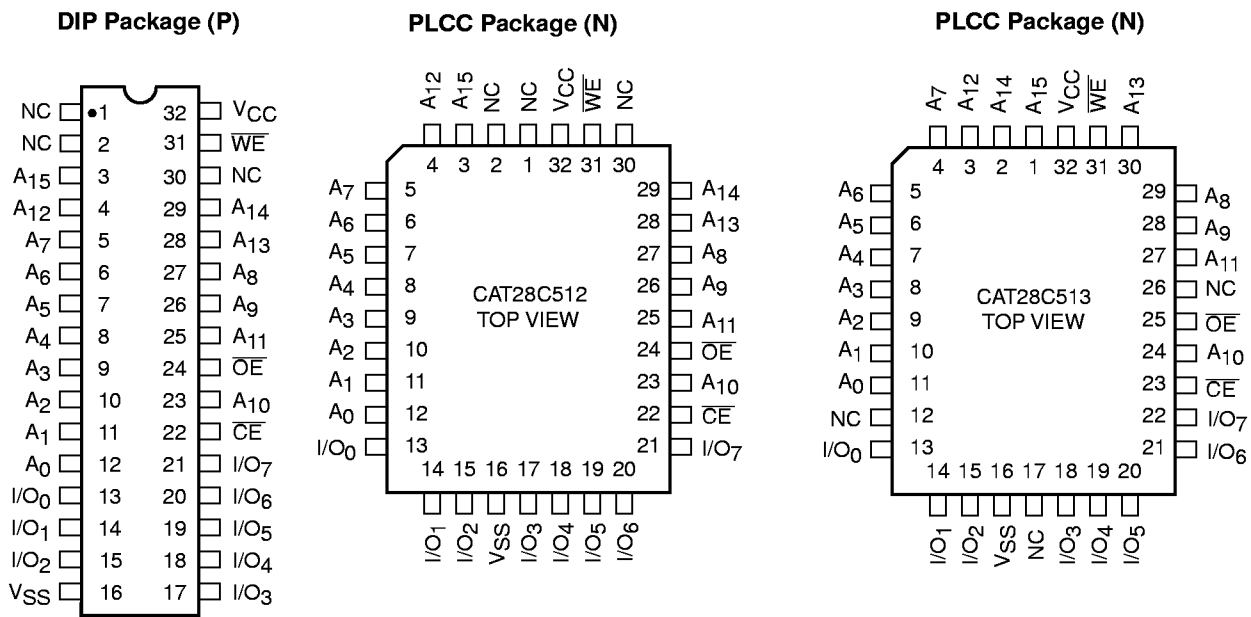




### PIN CONFIGURATION



5096 FHD F01

### TSOP Package (10mm X 14mm) (T14)



### PIN FUNCTIONS

Pin Name	Function	Pin Name	Function
A <sub>0</sub> -A <sub>15</sub>	Address Inputs	$\overline{WE}$	Write Enable
I/O <sub>0</sub> -I/O <sub>7</sub>	Data Inputs/Outputs	V <sub>CC</sub>	5V Supply
$\overline{CE}$	Chip Enable	V <sub>SS</sub>	Ground
$\overline{OE}$	Output Enable	NC	No Connect

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias ..... -55°C to +125°C  
 Storage Temperature ..... -65°C to +150°C  
 Voltage on Any Pin with  
     Respect to Ground<sup>(2)</sup> ..... -2.0V to +V<sub>CC</sub> + 2.0V  
 V<sub>CC</sub> with Respect to Ground ..... -2.0V to +7.0V  
 Package Power Dissipation  
     Capability (Ta = 25°C) ..... 1.0W  
 Lead Soldering Temperature (10 secs) ..... 300°C  
 Output Short Circuit Current<sup>(3)</sup> ..... 100 mA

**\*COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

**RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Min.	Max.	Units	Test Method
N <sub>END</sub> <sup>(1)</sup>	Endurance	10 <sup>4</sup> or 10 <sup>5</sup>		Cycles/Byte	MIL-STD-883, Test Method 1033
T <sub>DR</sub> <sup>(1)</sup>	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V <sub>ZAP</sub> <sup>(1)</sup>	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I <sub>LTH</sub> <sup>(1)(4)</sup>	Latch-Up	100		mA	JEDEC Standard 17

**D.C. OPERATING CHARACTERISTICS**



V<sub>CC</sub> = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Operating, TTL)			50	mA	$\overline{CE} = \overline{OE} = V_{IL}$ , f=8MHz All I/O's Open
I <sub>CCC</sub> <sup>(5)</sup>	V <sub>CC</sub> Current (Operating, CMOS)			25	mA	$\overline{CE} = \overline{OE} = V_{ILC}$ , f=8MHz All I/O's Open
I <sub>SB</sub>	V <sub>CC</sub> Current (Standby, TTL)			3	mA	$\overline{CE} = V_{IH}$ , All I/O's Open
I <sub>SBC</sub> <sup>(6)</sup>	V <sub>CC</sub> Current (Standby, CMOS)			500	μA	$\overline{CE} = V_{IHC}$ , All I/O's Open
I <sub>LI</sub>	Input Leakage Current	-10		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current	-10		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IH</sub> <sup>(6)</sup>	High Level Input Voltage	2		V <sub>CC</sub> + 0.3	V	
V <sub>IL</sub> <sup>(5)</sup>	Low Level Input Voltage	-1		0.8	V	
V <sub>OH</sub>	High Level Output Voltage	2.4			V	I <sub>OH</sub> = -400μA
V <sub>OL</sub>	Low Level Output Voltage			0.4	V	I <sub>OL</sub> = 2.1mA
V <sub>WI</sub>	Write Inhibit Voltage	3.5			V	

Note:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> + 0.5V, which may overshoot to V<sub>CC</sub> + 2.0V for periods of less than 20 ns.
- (3) Output shorted for no more than one second. No more than one output shorted at a time.
- (4) Latch-up protection is provided for stresses up to 100mA on address and data pins from -1V to V<sub>CC</sub> + 1V.
- (5) V<sub>ILC</sub> = -0.3V to +0.3V.
- (6) V<sub>IHC</sub> = V<sub>CC</sub> - 0.3V to V<sub>CC</sub> + 0.3V.

## MODE SELECTION

Mode	$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O	Power
Read	L	H	L	D <sub>OUT</sub>	ACTIVE
Byte Write ( $\overline{\text{WE}}$ Controlled)	L		H	D <sub>IN</sub>	ACTIVE
Byte Write ( $\overline{\text{CE}}$ Controlled)		L	H	D <sub>IN</sub>	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ ,  $V_{CC} = 5\text{V}$ 

Symbol	Test	Max.	Units	Conditions
$C_{I/O}^{(1)}$	Input/Output Capacitance	10	pF	$V_{I/O} = 0\text{V}$
$C_{IN}^{(1)}$	Input Capacitance	6	pF	$V_{IN} = 0\text{V}$

## A.C. CHARACTERISTICS, Read Cycle

 $V_{CC} = 5\text{V} \pm 10\%$ , Unless otherwise specified

Symbol	Parameter	28C512/513-12		28C512/513-15		28C512/513-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	120		150		200		ns
$t_{CE}$	$\overline{\text{CE}}$ Access Time		120		150		200	ns
$t_{AA}$	Address Access Time		120		150		200	ns
$t_{OE}$	$\overline{\text{OE}}$ Access Time		50		50		50	ns
$t_{LZ}^{(1)}$	$\overline{\text{CE}}$ Low to Active Output	0		0		0		ns
$t_{OLZ}^{(1)}$	$\overline{\text{OE}}$ Low to Active Output	0		0		0		ns
$t_{HZ}^{(1)(2)}$	$\overline{\text{CE}}$ High to High-Z Output		50		50		50	ns
$t_{OHZ}^{(1)(2)}$	$\overline{\text{OE}}$ High to High-Z Output		50		50		50	ns
$t_{OH}^{(1)}$	Output Hold from Address Change	0		0		0		ns

## Power-Up Timing

Symbol	Parameter	MAX	Units
$t_{PUR}^{(1)}$	Power-up to Read Operation	100	$\mu\text{s}$
$t_{PUW}^{(2)}$	Power-up to Write Operation	5	ms

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

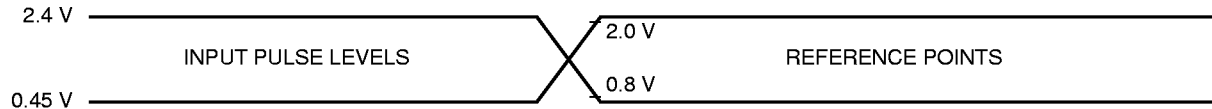
(2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.

**A.C. CHARACTERISTICS, Write Cycle**

V<sub>CC</sub>=5V±10%, unless otherwise specified

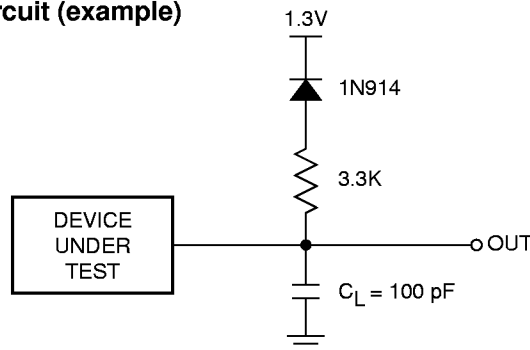
Symbol	Parameter	28C512/513-12		28C512/513-15		28C512/513-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time		5		5		5	ms
t <sub>AS</sub>	Address Setup Time	0		0		0		ns
t <sub>AH</sub>	Address Hold Time	50		50		50		ns
t <sub>CS</sub>	$\overline{CE}$ Setup Time	0		0		0		ns
t <sub>CH</sub>	$\overline{CE}$ Hold Time	0		0		0		ns
t <sub>CW</sub> <sup>(3)</sup>	$\overline{CE}$ Pulse Time	100		100		100		ns
t <sub>OES</sub>	$\overline{OE}$ Setup Time	0		0		0		ns
t <sub>OEH</sub>	$\overline{OE}$ Hold Time	0		0		0		ns
t <sub>WP</sub> <sup>(3)</sup>	$\overline{WE}$ Pulse Width	100		100		100		ns
t <sub>DS</sub>	Data Setup Time	50		50		50		ns
t <sub>DH</sub>	Data Hold Time	0		0		0		ns
t <sub>INIT</sub> <sup>(1)</sup>	Write Inhibit Period After Power-up	5	10	5	10	5	10	ms
t <sub>BLC</sub> <sup>(1)(4)</sup>	Byte Load Cycle Time	0.1	100	0.1	100	0.1	100	μs

**Figure 1. A.C. Testing Input/Output Waveform(2)**



5096 FHD F03

**Figure 2. A.C. Testing Load Circuit (example)**



5096 FHD F04

C<sub>L</sub> INCLUDES JIG CAPACITANCE

Note:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) Input rise and fall times (10% and 90%) < 10 ns.
- (3) A write pulse of less than 20ns duration will not initiate a write cycle.
- (4) A timer of duration t<sub>BLC</sub> max. begins with every LOW to HIGH transition of WE. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t<sub>BLC</sub> max. stops the timer.

### DEVICE OPERATION

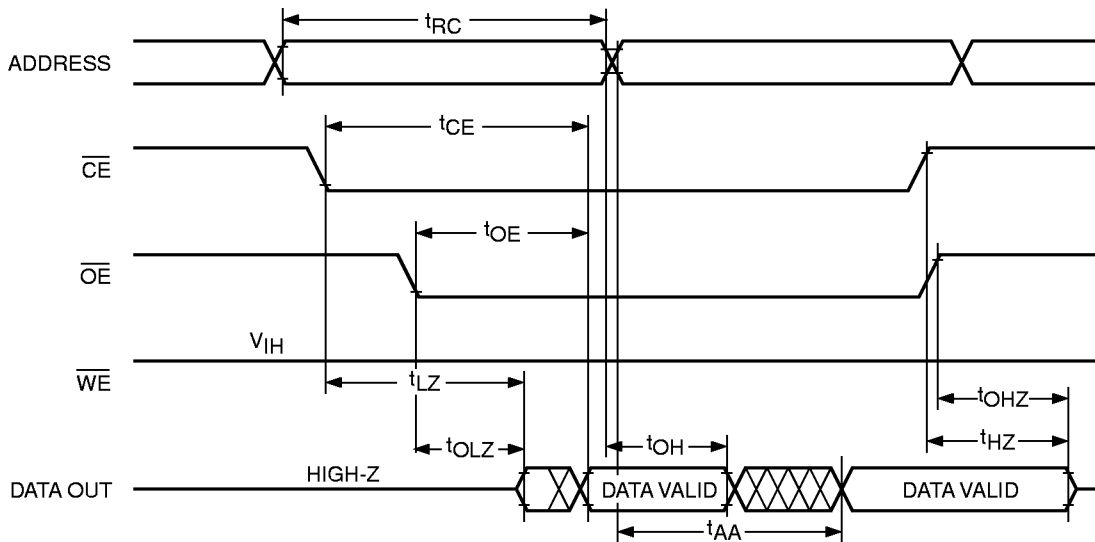
#### Read

Data stored in the CAT28C512/513 is transferred to the data bus when  $\overline{WE}$  is held high, and both  $\overline{OE}$  and  $\overline{CE}$  are held low. The data bus is set to a high impedance state when either  $\overline{CE}$  or  $\overline{OE}$  goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

#### Byte Write

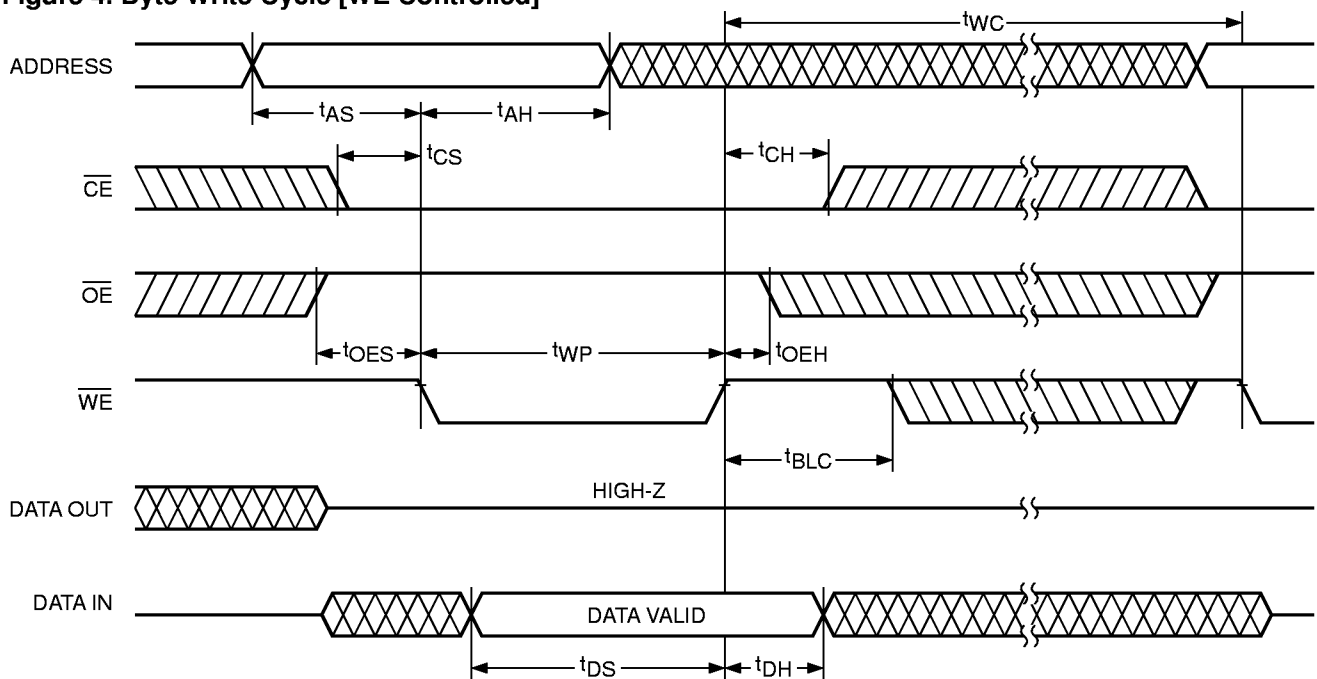
A write cycle is executed when both  $\overline{CE}$  and  $\overline{WE}$  are low, and  $\overline{OE}$  is high. Write cycles can be initiated using either  $\overline{WE}$  or  $\overline{CE}$ , with the address input being latched on the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever occurs last. Data, conversely, is latched on the rising edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 5 ms.

Figure 3. Read Cycle



28C512/513 F06

Figure 4. Byte Write Cycle [ $\overline{WE}$  Controlled]



5096 FHD F06

**Page Write**

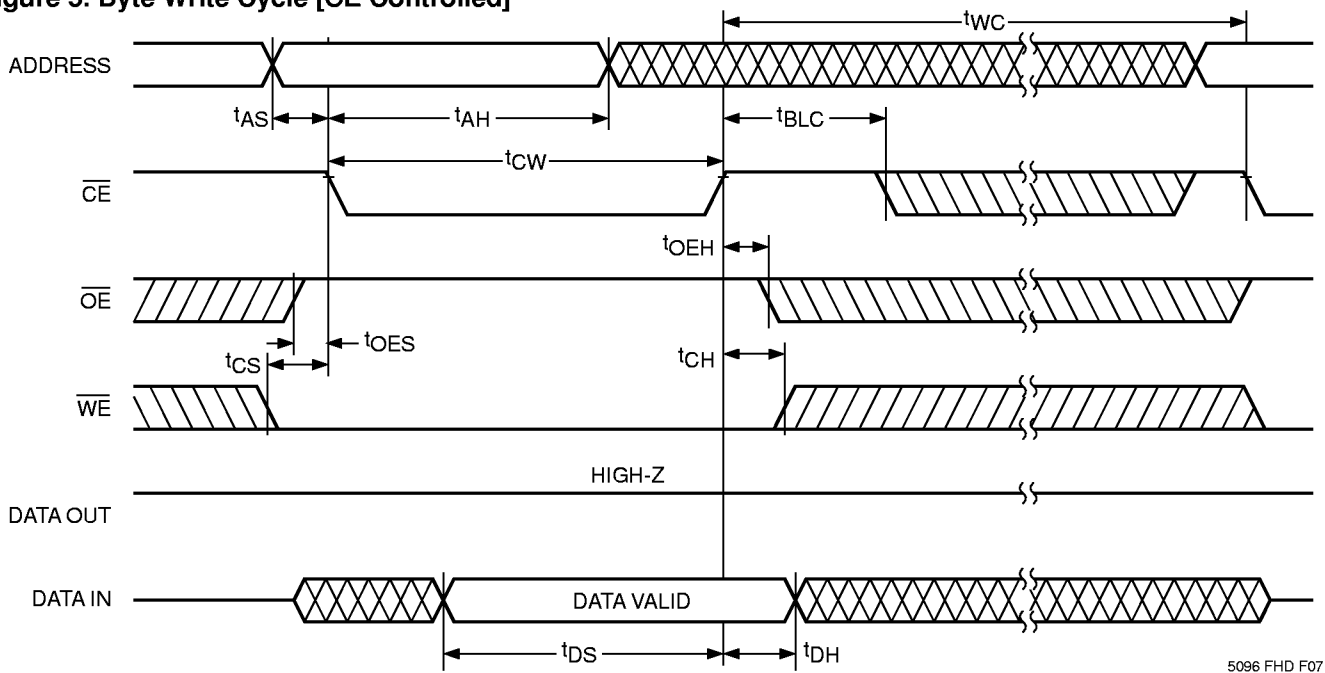
The page write mode of the CAT28C512/513 (essentially an extended BYTE WRITE mode) allows from 1 to 128 bytes of data to be programmed within a single E<sup>2</sup>PROM write cycle. This effectively reduces the byte-write time by a factor of 128.

Following an initial WRITE operation ( $\overline{WE}$  pulsed low, for  $t_{WP}$ , and then high) the page write mode can begin by issuing sequential  $\overline{WE}$  pulses, which load the address and data bytes into a 128 byte temporary buffer. The page address where data is to be written, specified by bits A<sub>7</sub> to A<sub>15</sub>, is latched on the last falling edge of  $\overline{WE}$ . Each byte within the page is defined by address bits A<sub>0</sub>

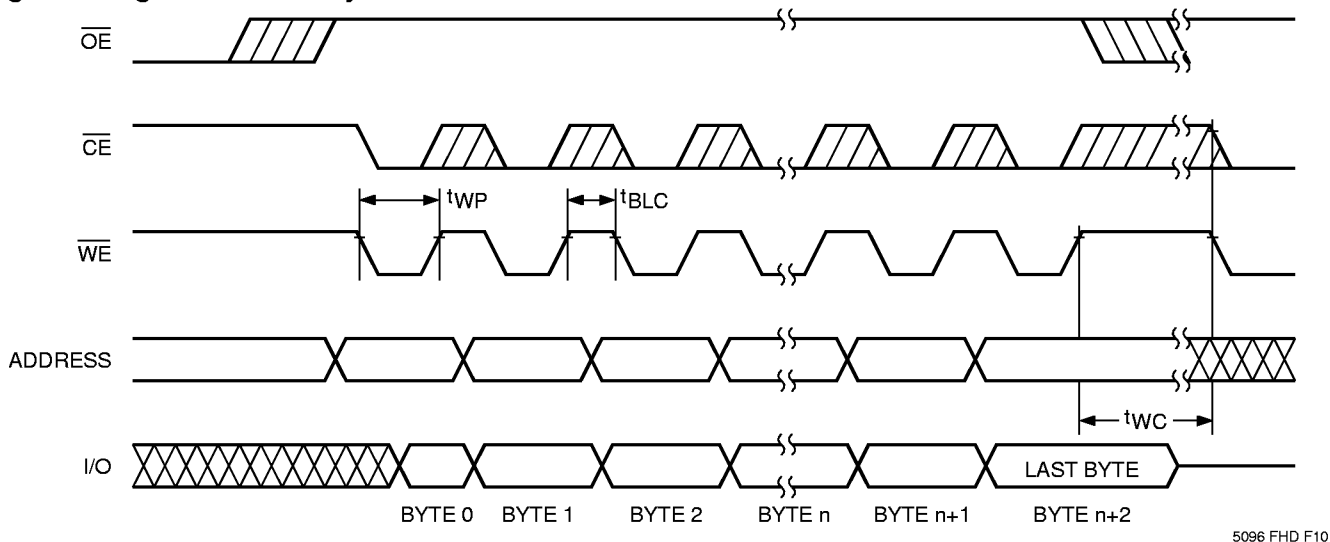
to A<sub>6</sub> (which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within  $t_{BLC\ MAX}$  of the rising edge of the preceding  $\overline{WE}$  pulse. There is no page write window limitation as long as  $\overline{WE}$  is pulsed low within  $t_{BLC\ MAX}$ .

Upon completion of the page write sequence,  $\overline{WE}$  must stay high a minimum of  $t_{BLC\ MAX}$  for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

**Figure 5. Byte Write Cycle [ $\overline{CE}$  Controlled]**



**Figure 6. Page Mode Write Cycle**



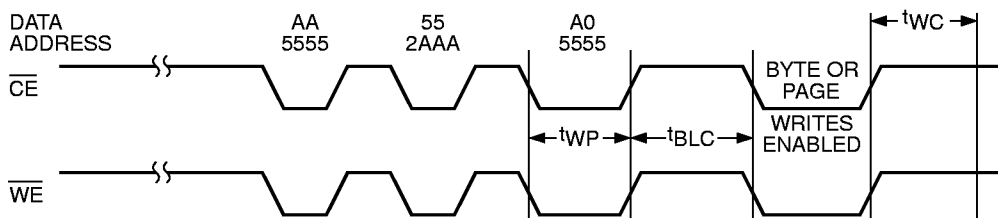




To activate the software data protection, the device must be sent three write commands to specific addresses with specific data (Figure 9). This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications (Figure 11). Once this is done, all subsequent byte or page writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued regardless of power on/off transitions. This gives the user added inadvertent write protection on power-up in addition to the hardware protection provided.

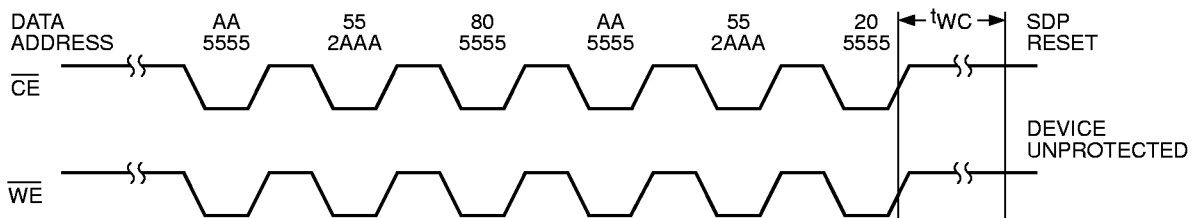
To allow the user the ability to program the device with an E<sup>2</sup>PROM programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (Figure 10) will reset the internal protection circuitry, and the device will return to standard operating mode (Figure 12 provides reset timing). After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

Figure 11. Software Data Protection Timing



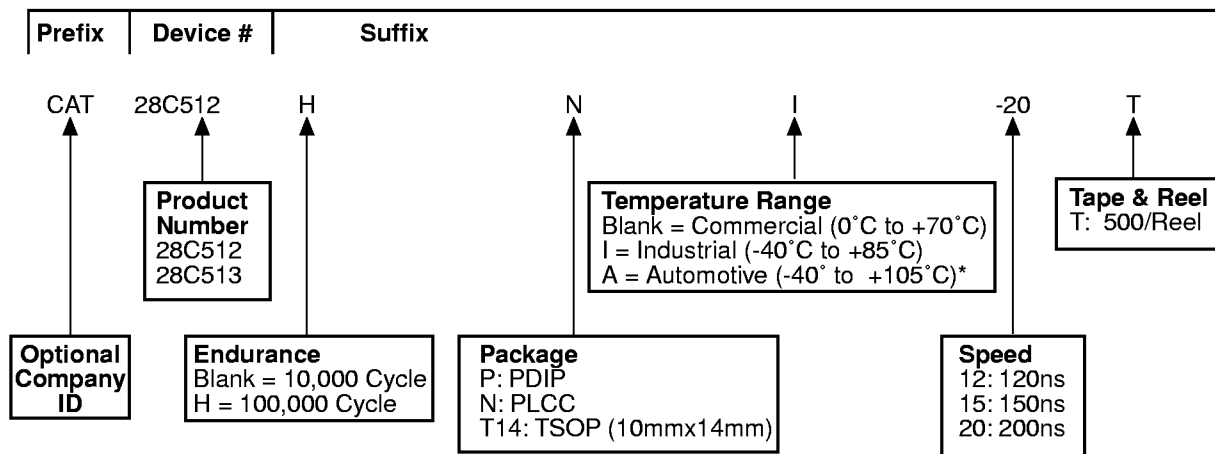
5096 FHD F13

Figure 12. Resetting Software Data Protection Timing



5096 FHD F14

ORDERING INFORMATION



\* -40°C to +125°C is available upon request

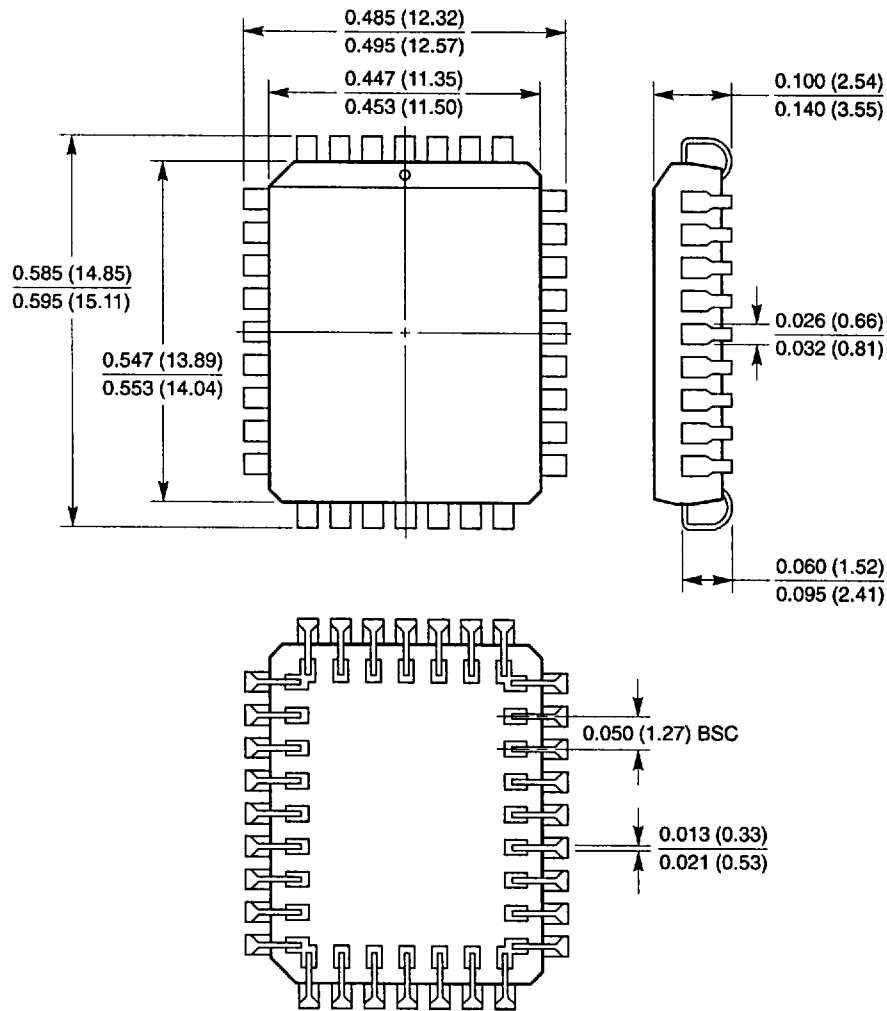
Notes:

- (1) The device used in the above example is a CAT28C512HNI-20T (100,000 Cycle Endurance, PLCC, Industrial temperature, 200 ns Access Time, Tape & Reel).
- (2) 28C513 is offered only in PLCC package.

28C512/513 F16



**32-LEAD PLASTIC LEADED CHIP CARRIER (N)**

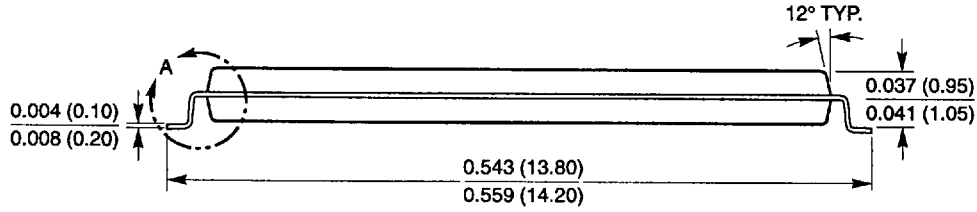
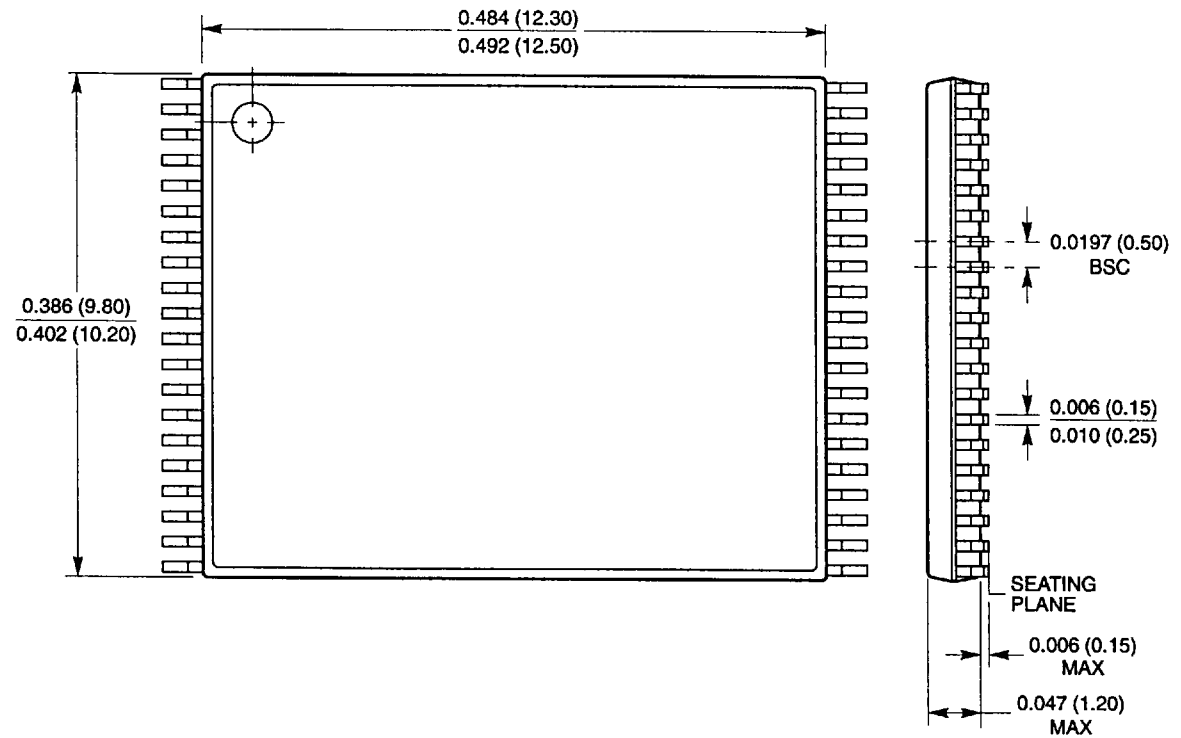


**Notes:**

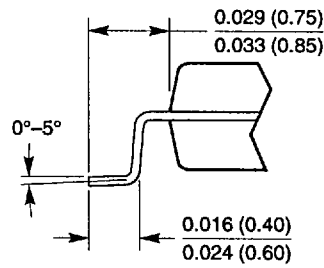
1. Complies with JEDEC Publication 95 MO-052 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.



40-LEAD 10MM X 14MM TSOP (T14)



DETAIL "A"

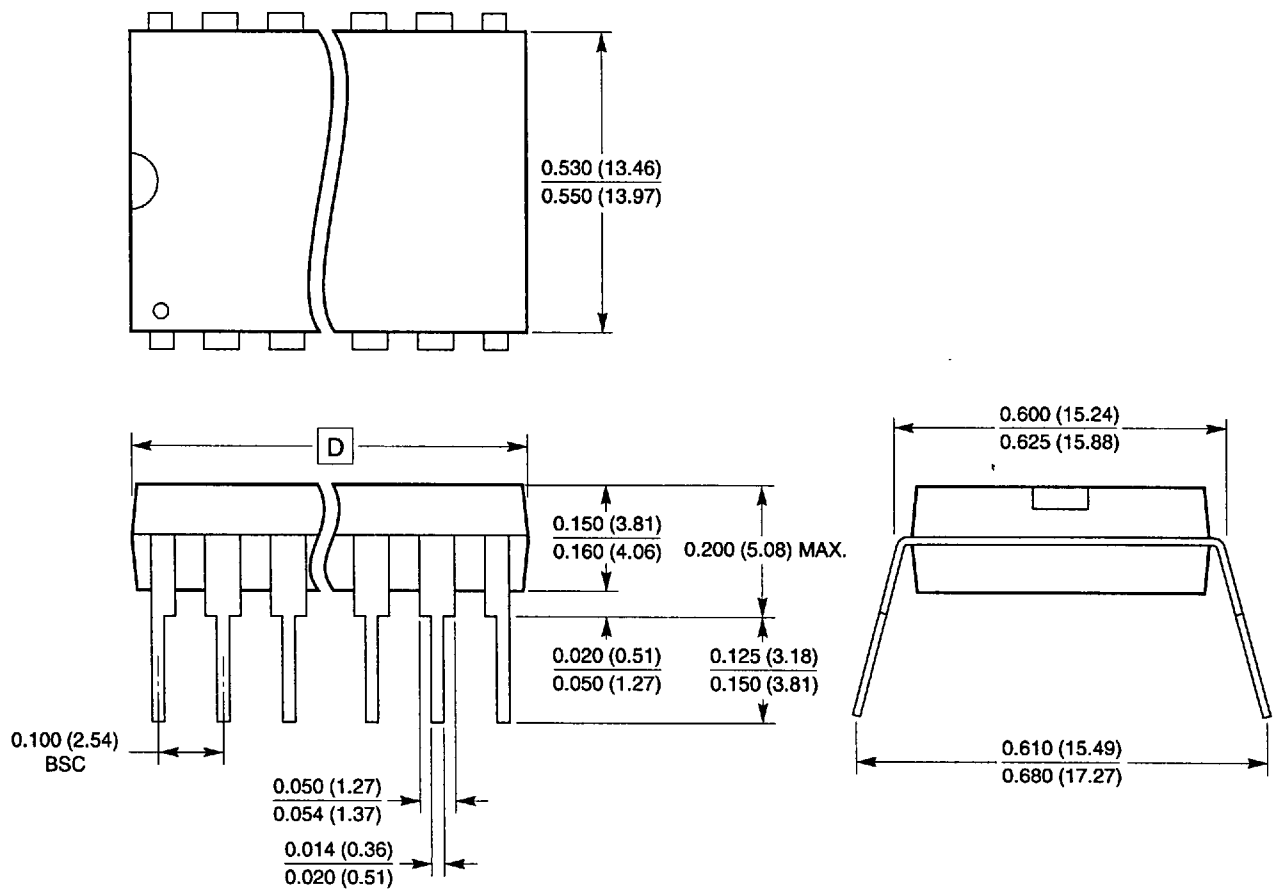


Note:

1. All linear dimensions are in inches and parenthetically in millimeters.



**24-40-LEAD 600 MIL WIDE PLASTIC DIP (P)**



Dimension D		
Pkg	Min	Max
24L	1.240 (31.50)	1.270 (32.25)
28L	1.420 (36.06)	1.470 (37.33)
32L	1.640 (41.65)	1.670 (42.41)
40L	2.040 (51.81)	2.070 (52.57)

**Notes:**

1. Complies with JEDEC Publication 95 MO-015 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.