



CAT28C256

256K-Bit CMOS PARALLEL E²PROM

FEATURES

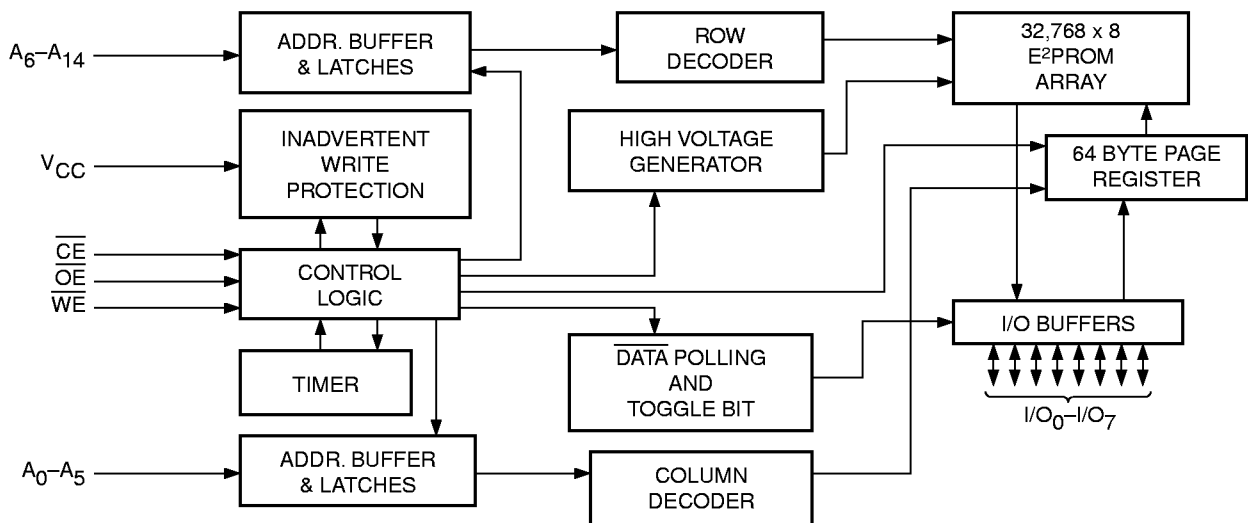
- Fast Read Access Times: 120/150/200 ns
- Low Power CMOS Dissipation:
 - Active: 25 mA Max.
 - Standby: 150 μ A Max.
- Simple Write Operation:
 - On-Chip Address and Data Latches
 - Self-Timed Write Cycle with Auto-Clear
- Fast Write Cycle Time:
 - 5ms Max
- CMOS and TTL Compatible I/O
- Hardware and Software Write Protection
- Automatic Page Write Operation:
 - 1 to 64 Bytes in 5ms
 - Page Load Timer
- End of Write Detection:
 - Toggle Bit
 - DATA Polling
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Commercial, Industrial and Automotive Temperature Ranges

DESCRIPTION

The CAT28C256 is a fast, low power, 5V-only CMOS parallel E²PROM organized as 32K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. DATA Polling and Toggle status bits signal the start and end of the self-timed write cycle. Additionally, the CAT28C256 features hardware and software write protection.

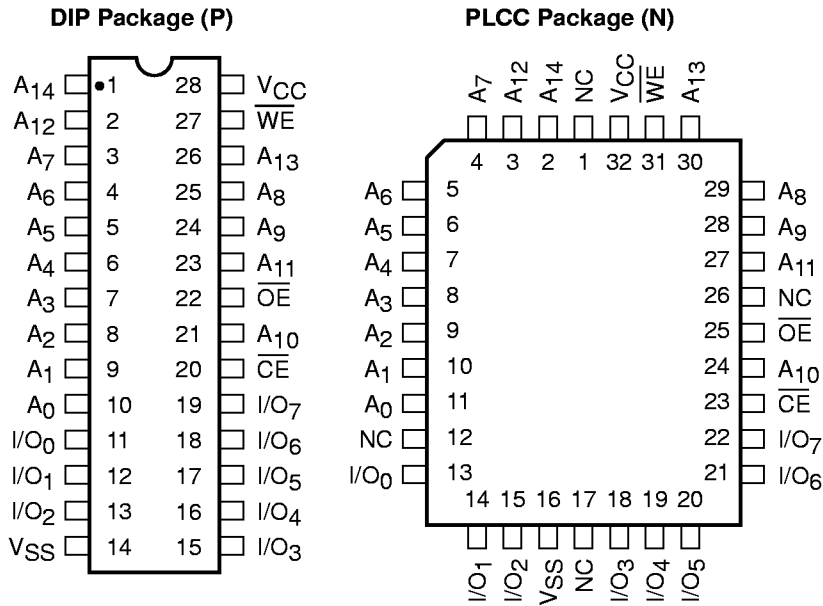
The CAT28C256 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in JEDEC approved 28-pin DIP, 28-pin TSOP or 32-pin PLCC packages.

BLOCK DIAGRAM



5096 FHD F02

PIN CONFIGURATION



5096 FHD F01

TSOP Package (8mm X 13.4mm) (T13)



28C256 F03

PIN FUNCTIONS

Pin Name	Function	Pin Name	Function
A0–A14	Address Inputs	WE	Write Enable
I/O0–I/O7	Data Inputs/Outputs	VCC	5V Supply
CE	Chip Enable	VSS	Ground
OE	Output Enable	NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground ⁽²⁾	-2.0V to +V _{CC} + 2.0V
V _{CC} with Respect to Ground	-2.0V to +7.0V
Package Power Dissipation Capability (Ta = 25°C)	1.0W
Lead Soldering Temperature (10 secs)	300°C
Output Short Circuit Current ⁽³⁾	100 mA

***COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N _{END} ⁽¹⁾	Endurance	10 ⁴ or 10 ⁵		Cycles/Byte	MIL-STD-883, Test Method 1033
T _{DR} ⁽¹⁾	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V _{ZAP} ⁽¹⁾	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I _{LTH} ⁽¹⁾⁽⁴⁾	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I _{CC}	V _{CC} Current (Operating, TTL)			30	mA	$\overline{CE} = \overline{OE} = V_{IL}$, f=8MHz All I/O's Open
I _{CCC} ⁽⁵⁾	V _{CC} Current (Operating, CMOS)			25	mA	$\overline{CE} = \overline{OE} = V_{ILC}$, f=8MHz All I/O's Open
I _{SB}	V _{CC} Current (Standby, TTL)			1	mA	$\overline{CE} = V_{IH}$, All I/O's Open
I _{SBC} ⁽⁶⁾	V _{CC} Current (Standby, CMOS)			150	μA	$\overline{CE} = V_{IHC}$, All I/O's Open
I _{LI}	Input Leakage Current	-10		10	μA	V _{IN} = GND to V _{CC}
I _{LO}	Output Leakage Current	-10		10	μA	V _{OUT} = GND to V _{CC} , $\overline{CE} = V_{IH}$
V _{IH} ⁽⁶⁾	High Level Input Voltage	2		V _{CC} + 0.3	V	
V _{IL} ⁽⁵⁾	Low Level Input Voltage	-0.3		0.8	V	
V _{OH}	High Level Output Voltage	2.4			V	I _{OH} = -400μA
V _{OL}	Low Level Output Voltage			0.4	V	I _{OL} = 2.1 mA
V _{WI}	Write Inhibit Voltage	3.5			V	

Note:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20 ns.
- (3) Output shorted for no more than one second. No more than one output shorted at a time.
- (4) Latch-up protection is provided for stresses up to 100mA on address and data pins from -1V to V_{CC} + 1V.
- (5) V_{ILC} = -0.3V to +0.3V.
- (6) V_{IHC} = V_{CC} - 0.3V to V_{CC} + 0.3V.

MODE SELECTION

Mode	\overline{CE}	\overline{WE}	\overline{OE}	I/O	Power
Read	L	H	L	D _{OUT}	ACTIVE
Byte Write (\overline{WE} Controlled)	L		H	D _{IN}	ACTIVE
Byte Write (\overline{CE} Controlled)		L	H	D _{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
C _{I/O} ⁽¹⁾	Input/Output Capacitance	10	pF	V _{I/O} = 0V
C _{IN} ⁽¹⁾	Input Capacitance	6	pF	V _{IN} = 0V

A.C. CHARACTERISTICS, Read Cycle

V_{CC}=5V ± 10%, Unless otherwise specified

Symbol	Parameter	28C256-12		28C256-15		28C256-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	120		150		200		ns
t _{CE}	\overline{CE} Access Time		120		150		200	ns
t _{AA}	Address Access Time		120		150		200	ns
t _{OE}	\overline{OE} Access Time		50		70		80	ns
t _{LZ} ⁽¹⁾	\overline{CE} Low to Active Output	0		0		0		ns
t _{OLZ} ⁽¹⁾	\overline{OE} Low to Active Output	0		0		0		ns
t _{HZ} ⁽¹⁾⁽²⁾	\overline{CE} High to High-Z Output		50		50		50	ns
t _{OHZ} ⁽¹⁾⁽²⁾	\overline{OE} High to High-Z Output		50		50		50	ns
t _{OH} ⁽¹⁾	Output Hold from Address Change	0		0		0		ns

Note:

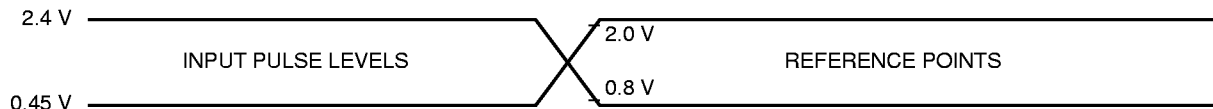
- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.

A.C. CHARACTERISTICS, Write Cycle

V_{CC}=5V±10%, unless otherwise specified

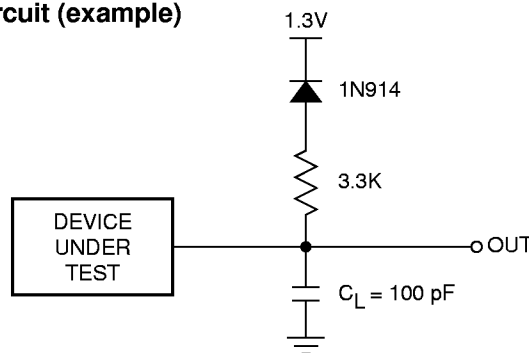
Symbol	Parameter	28C256-12		28C256-15		28C256-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{wc}	Write Cycle Time		5		5		5	ms
t _{AS}	Address Setup Time	0		0		0		ns
t _{AH}	Address Hold Time	50		50		50		ns
t _{CS}	\overline{CE} Setup Time	0		0		0		ns
t _{CH}	\overline{CE} Hold Time	0		0		0		ns
t _{cw} ⁽³⁾	\overline{CE} Pulse Time	100		100		100		ns
t _{oES}	\overline{OE} Setup Time	0		0		0		ns
t _{oEH}	\overline{OE} Hold Time	0		0		0		ns
t _{wP} ⁽³⁾	\overline{WE} Pulse Width	100		100		100		ns
t _{DS}	Data Setup Time	50		50		50		ns
t _{DH}	Data Hold Time	10		10		10		ns
t _{INIT} ⁽¹⁾	Write Inhibit Period After Power-up	5	10	5	10	5	10	ms
t _{BLC} ⁽¹⁾⁽⁴⁾	Byte Load Cycle Time	0.1	100	0.1	100	0.1	100	μs

Figure 1. A.C. Testing Input/Output Waveform(2)



5096 FHD F03

Figure 2. A.C. Testing Load Circuit (example)



5096 FHD F04

Note:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) Input rise and fall times (10% and 90%) < 10 ns.
- (3) A write pulse of less than 20ns duration will not initiate a write cycle.
- (4) A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of WE. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.

DEVICE OPERATION

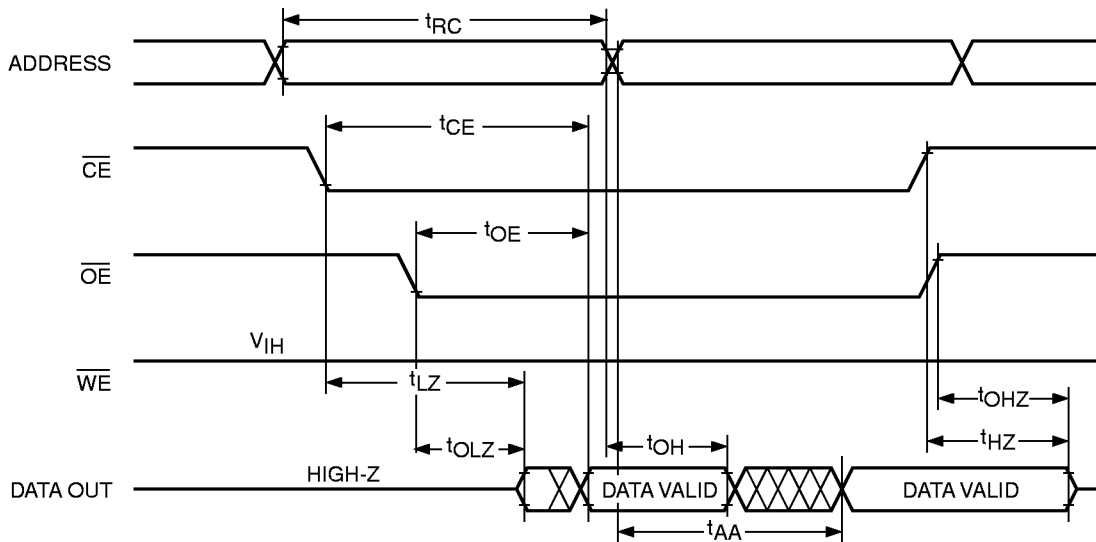
Read

Data stored in the CAT28C256 is transferred to the data bus when \overline{WE} is held high, and both \overline{OE} and \overline{CE} are held low. The data bus is set to a high impedance state when either \overline{CE} or \overline{OE} goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

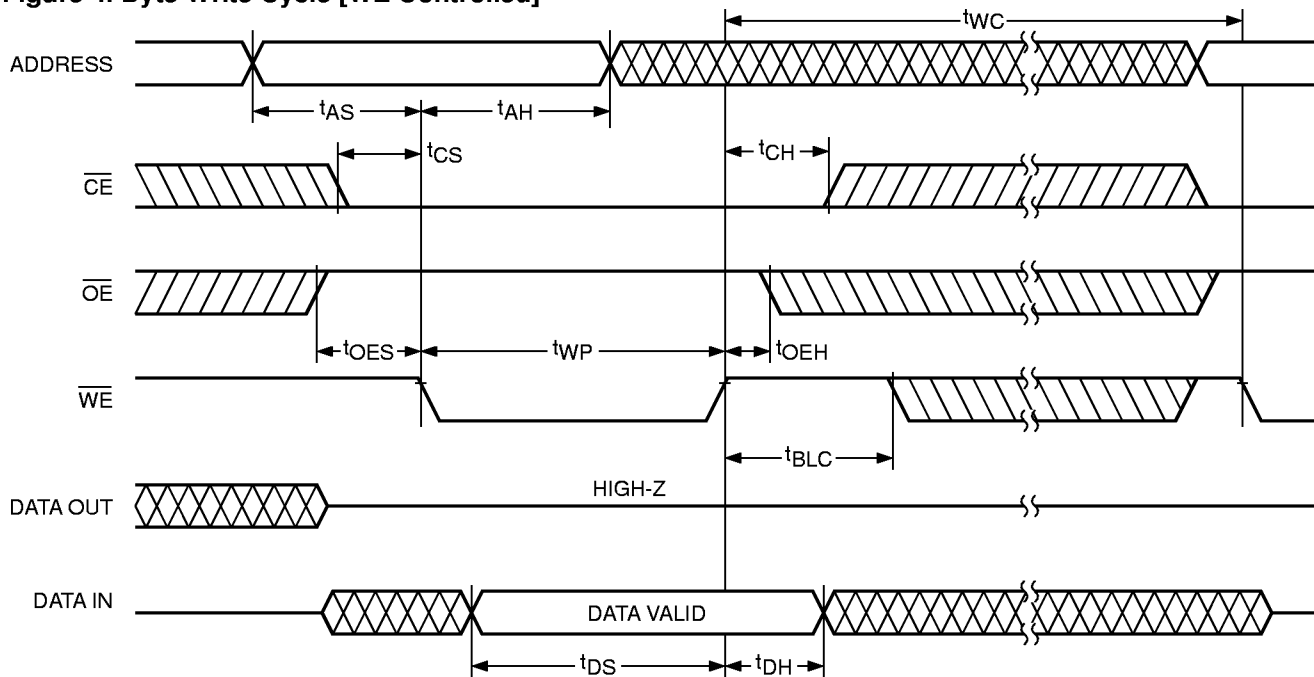
A write cycle is executed when both \overline{CE} and \overline{WE} are low, and \overline{OE} is high. Write cycles can be initiated using either \overline{WE} or \overline{CE} , with the address input being latched on the falling edge of \overline{WE} or \overline{CE} , whichever occurs last. Data, conversely, is latched on the rising edge of \overline{WE} or \overline{CE} , whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 5 ms.

Figure 3. Read Cycle



28C256 F06

Figure 4. Byte Write Cycle [\overline{WE} Controlled]



5096 FHD F06

Page Write

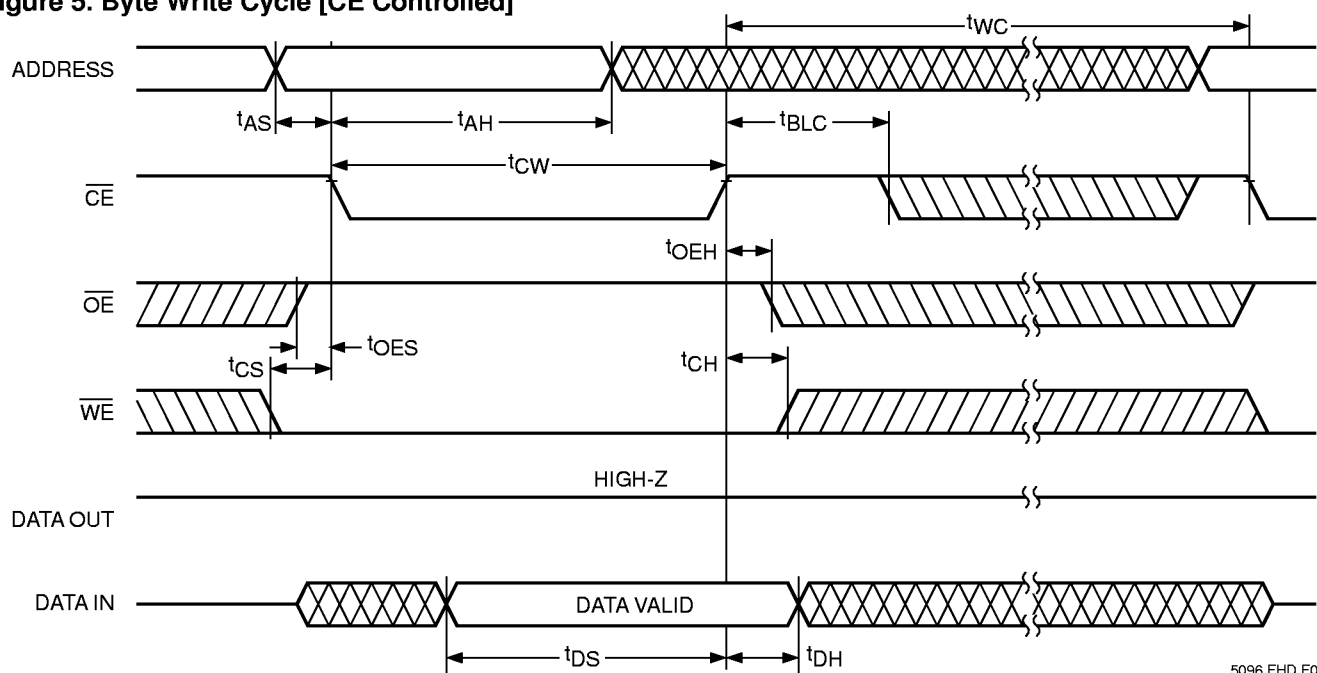
The page write mode of the CAT28C256 (essentially an extended BYTE WRITE mode) allows from 1 to 64 bytes of data to be programmed within a single E²PROM write cycle. This effectively reduces the byte-write time by a factor of 64.

Following an initial WRITE operation (\overline{WE} pulsed low, for t_{WP} , and then high) the page write mode can begin by issuing sequential \overline{WE} pulses, which load the address and data bytes into a 64 byte temporary buffer. The page address where data is to be written, specified by bits A_6 to A_{14} , is latched on the last falling edge of \overline{WE} . Each byte within the page is defined by address bits A_0 to A_5

(which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\ MAX}$ of the rising edge of the preceding \overline{WE} pulse. There is no page write window limitation as long as \overline{WE} is pulsed low within $t_{BLC\ MAX}$.

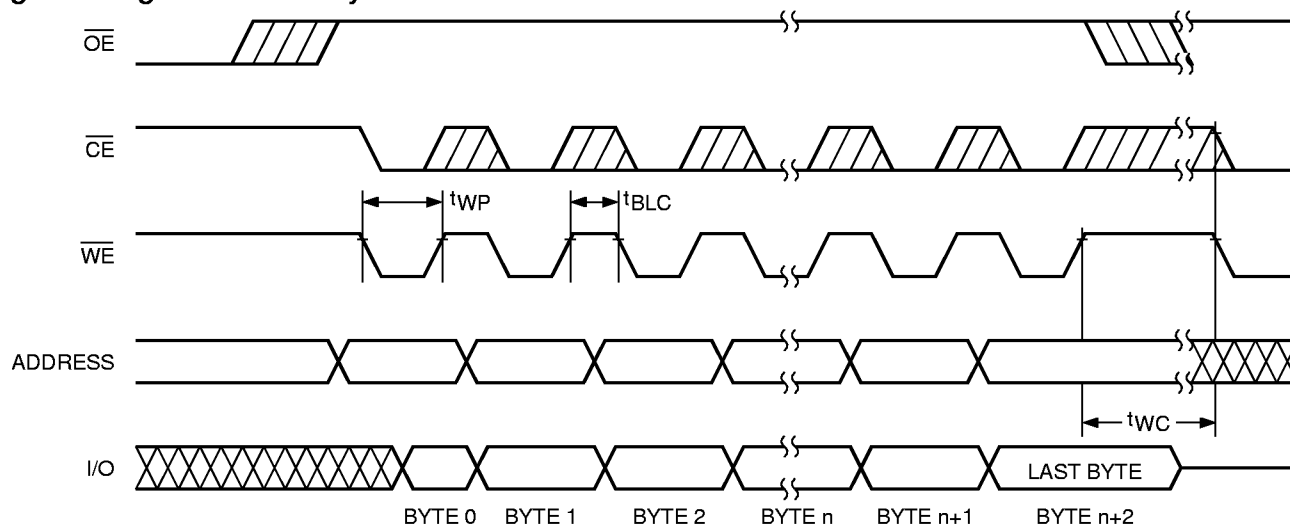
Upon completion of the page write sequence, \overline{WE} must stay high a minimum of $t_{BLC\ MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

Figure 5. Byte Write Cycle [\overline{CE} Controlled]



5096 FHD F07

Figure 6. Page Mode Write Cycle



5096 FHD F10

HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C256.

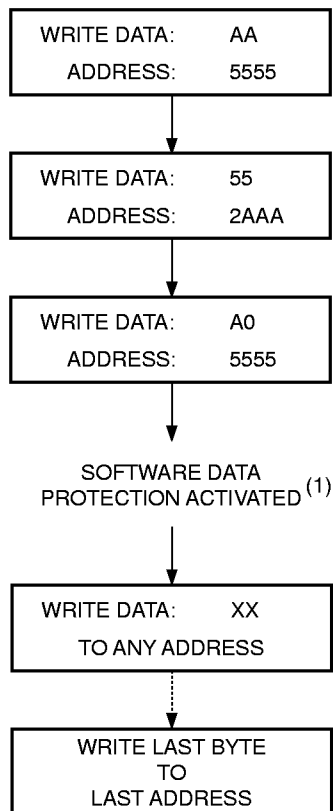
- (1) V_{CC} sense provides for write protection when V_{CC} falls below 3.5V min.
- (2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after V_{CC} has reached 3.5V min.
- (3) Write inhibit is activated by holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high.

- (4) Noise pulses of less than 20 ns on the \overline{WE} or \overline{CE} inputs will not result in a write cycle.

SOFTWARE DATA PROTECTION

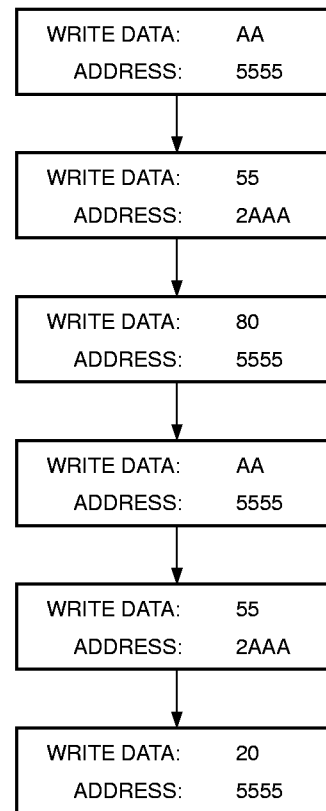
The CAT28C256 features a software controlled data protection scheme which, once enabled, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from Catalyst with the software protection NOT ENABLED (the CAT28C256 is in the standard operating mode).

Figure 9. Write Sequence for Activating Software Data Protection



5096 FHD F08

Figure 10. Write Sequence for Deactivating Software Data Protection



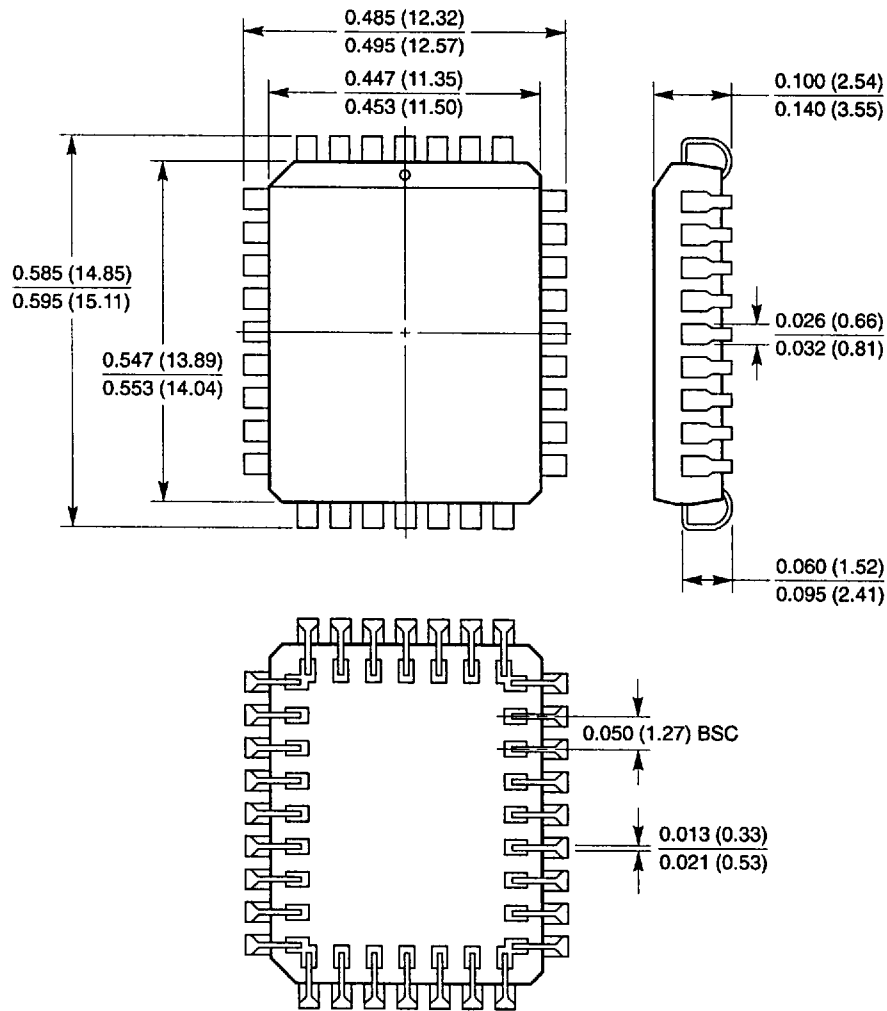
5096 FHD F09

Note:

- (1) Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within t_{BLC} Max., after SDP activation.



32-LEAD PLASTIC LEADED CHIP CARRIER (N)

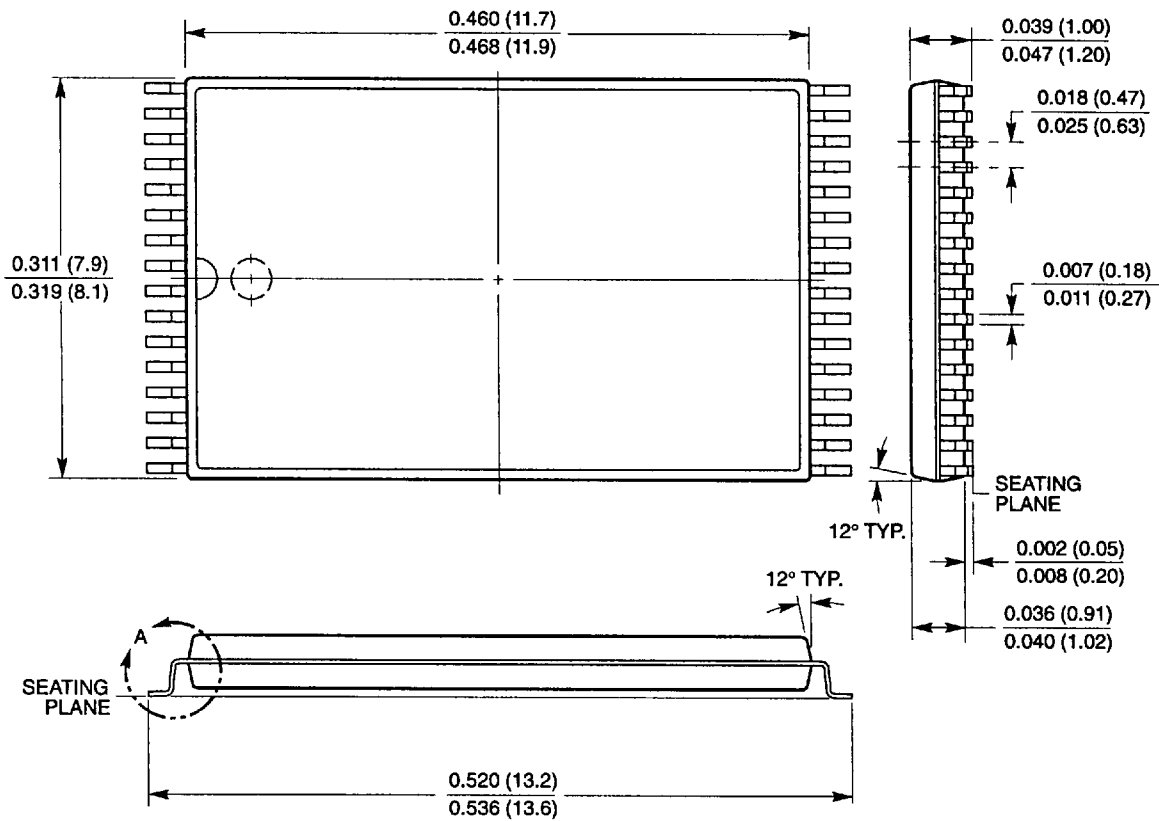


Notes:

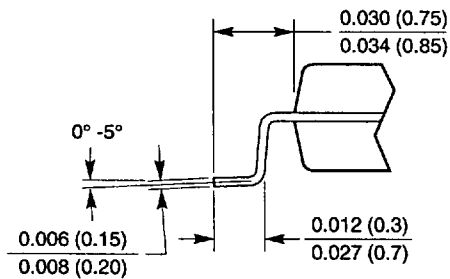
1. Complies with JEDEC Publication 95 MO-052 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.



28-LEAD 8MM X 13.4 MM TSOP (T13)



DETAIL "A"

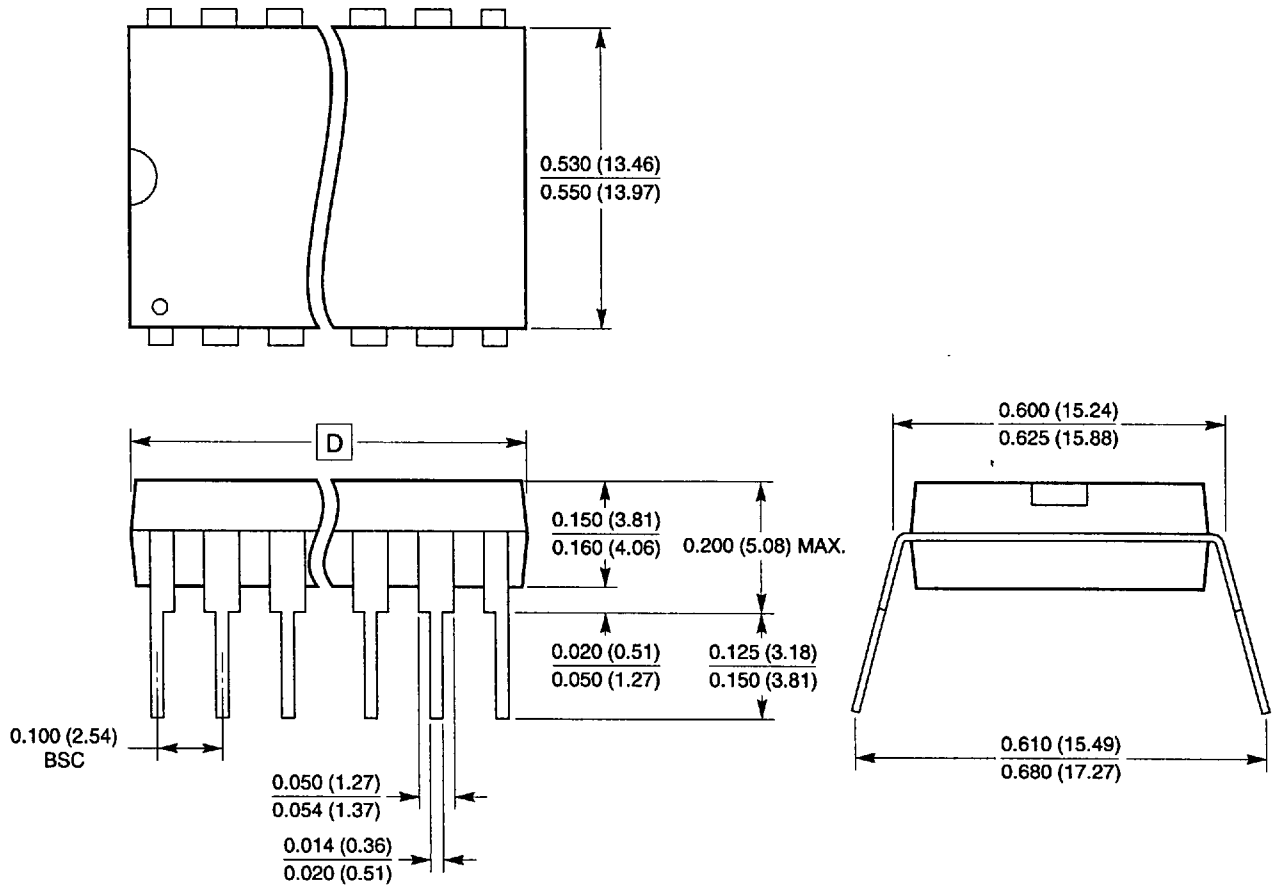


Notes:

1. All linear dimensions are in inches and parenthetically in millimeters.



24-40-LEAD 600 MIL WIDE PLASTIC DIP (P)



Dimension D		
Pkg	Min	Max
24L	1.240 (31.50)	1.270 (32.25)
28L	1.420 (36.06)	1.470 (37.33)
32L	1.640 (41.65)	1.670 (42.41)
40L	2.040 (51.81)	2.070 (52.57)

Notes:

1. Complies with JEDEC Publication 95 MO-015 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.