

CAT28C16V3 2K x 8 BIT CMOS POWER MISER™ E²PROM

PRELIMINARY

DESCRIPTION

The CAT28C16V3 is a fast, low power, 3V-only CMOS E²PROM requiring a simple interface for in-system programming.

On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Data polling is provided to allow the user to minimize write cycle time.

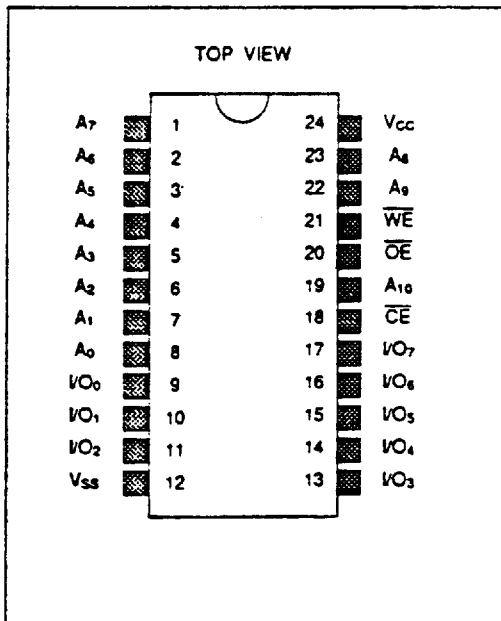
The CAT28C16V3 is fabricated in reliable floating gate CMOS technology. It is designed for up to 10,000 write cycles and 10 years data retention.

FEATURES

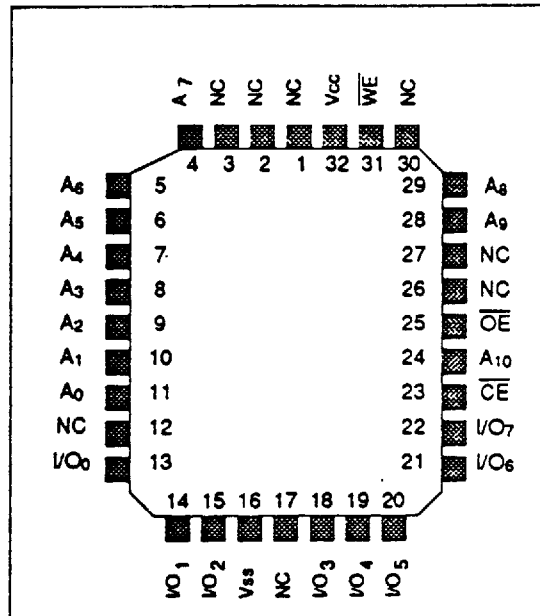
- Access time: 700ns
- Low CMOS power:
 - Active: 10mA max
 - Standby: 50µA max
- 3V-only operation
- Simple write operation:
 - On-chip address and data latches
 - Self-timed write cycle with auto-erase
 - Data polling
 - Power up/down write protection
- 20 ms max nonvolatile write cycle
- Reliable floating gate CMOS technology
- JEDEC approved 24-pin DIP, Small Outline, and 32-pin PLCC packages available
- Power-up inadvertent write protection

PIN CONFIGURATION

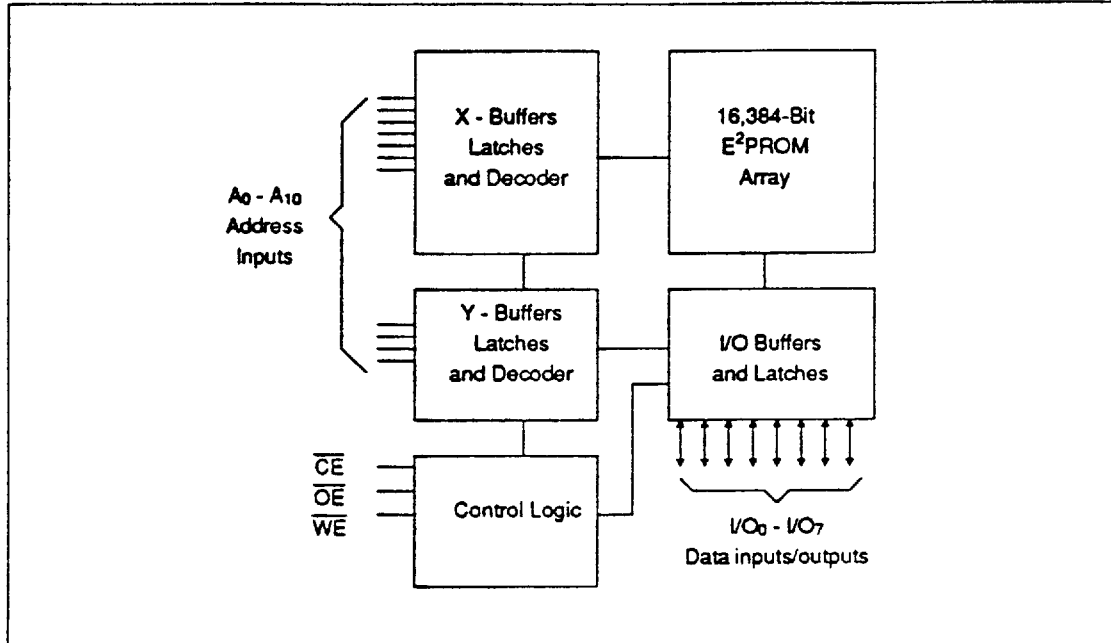
24-Pin DIP and S.O.



32-Pin PLCC



BLOCK DIAGRAM



PIN NAMES

A ₀ - A ₁₀	Address inputs
I/O ₀ - I/O ₇	Data inputs/outputs
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable
$\overline{\text{WE}}$	Write enable
V _{cc}	+3V
V _{ss}	Ground

CAPACITANCE

(T_A = 25°C, f = 1.0MHz, V_{cc} = 3V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
C _{IO}	Input/Output capacitance	V _{IO} = 0V	10	pF
C _{IN}	Input capacitance	V _{IN} = 0V	6	pF

Note: These parameters are periodically sampled and are not 100% tested.

ABSOLUTE MAXIMUM RATINGS *

Temperature under bias	-40°C to +85°C
Storage temperature	-65°C to +150°C
Voltage on any input pin relative to V _{SS}	-0.5 to +7V
Voltage on any output pin relative to V _{SS}	-0.5 to V _{CC} +0.5V
D.C. output current	5mA


*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +3V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{CC}	V _{CC} current (operating, TTL)	$\overline{CE}=\overline{OE}=V_{IL}$, f=4.0MHz, all I/O's = open			10	mA
I _{SB}	V _{CC} current (standby, TTL)	$\overline{CE}=V_{IH}$ All I/O's open			50	μA
I _{LI}	Input leakage current	V _{IN} = GND to V _{CC}			10	μA
I _{LO}	Output leakage current	V _{OUT} = GND to V _{CC} , $\overline{CE} = V_{IH}$			10	μA
V _{IH}	High level input voltage		V _{CC} -0.3		V _{CC} +1	V
V _{IL}	Low level input voltage		-0.3		0.3	V
V _{OH}	High level output voltage	I _{OH} = -10μA	V _{CC} -0.3			V
V _{OL}	Low level output voltage	I _{OL} = 10μA			0.3	V
V _{WI}	V _{CC} trip voltage for write protection		2.0	2.5		V

MODE SELECTION

Mode	\overline{CE}	\overline{WE}	\overline{OE}	I/O	Power
Read	L	H	L	D _{OUT}	ACTIVE
Byte write	L		H	D _{IN}	ACTIVE
Standby and write inhibit	H	X	X	High-Z	STANDBY
Write inhibit	X	X	L		
Write inhibit	X	H	X		
Chip erase	L	L	12V	High-Z	ACTIVE

AC CHARACTERISTICS - TEST CONDITIONS

Parameter	Conditions
Input pulse level	0 to V _{CC}
Input rise and fall times	10ns
Input/output timing reference level	1.5V
Output load	C _L = 100pF, 1 TTL gate

AC CHARACTERISTICS <Read Cycle>

(V_{CC} = +3V ±10%, T_A = 0°C TO +70°C)

Symbol	Parameter	28C16V3-70		Units
t _{RC}	Read Cycle Time	700		ns
t _{CE}	\overline{CE} Access Time		700	ns
t _{AA}	Address Access Time		700	ns
t _{OE}	\overline{OE} Access Time		450	ns
t _{LZ}	\overline{CE} Low to Active Output	10		ns
t _{OLZ}	\overline{OE} Low to Active Output	10		ns
t _{HZ}	\overline{CE} High to High-z Output	10	80	ns
t _{OHZ}	\overline{OE} High to High-z Output	10	80	ns
t _{OH}	Output Hold from Address Change	100		ns

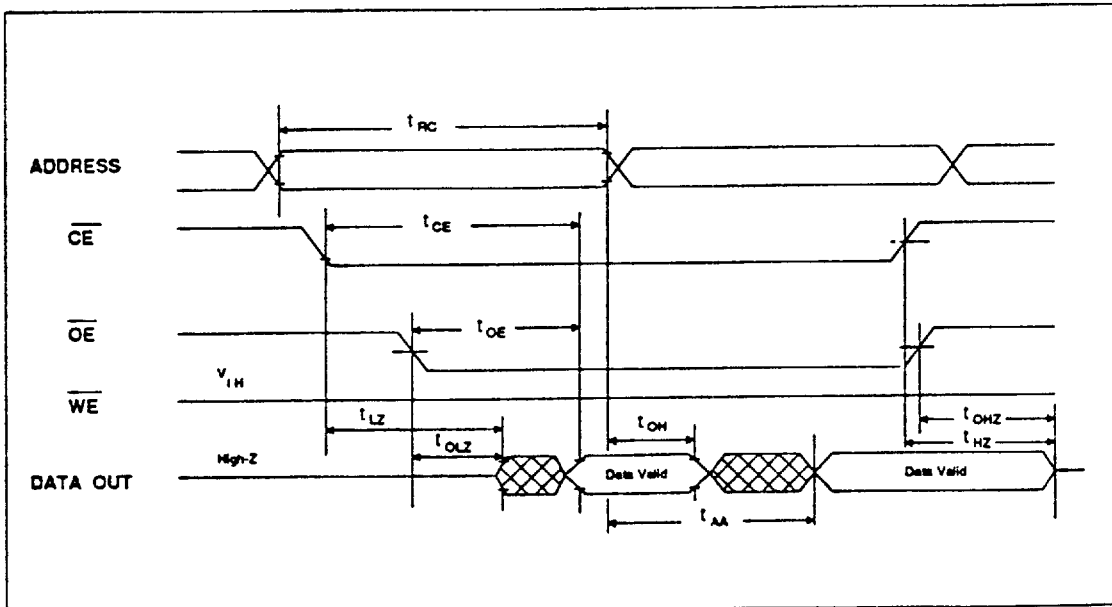
AC CHARACTERISTICS <Write Cycle>

($V_{CC} = +3V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$)

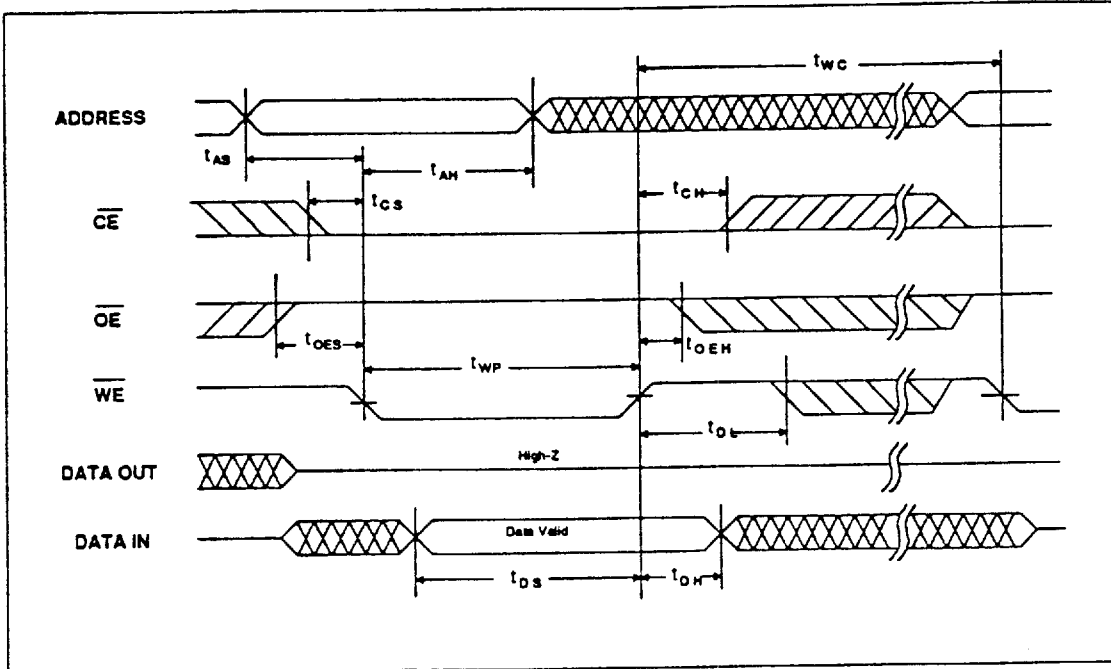
Symbol	Parameter	28C16V3-70		Units
		Min.	Max.	
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	150		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	\overline{CE} Pulse Time	200		ns
$t_{OES}, t_{OE H}$	\overline{OE} Setup Time, \overline{OE} Hold Time	100		ns
t_{WP}	\overline{WE} Pulse Width	200		ns
t_{DL}	Data Latch Time	100		ns
t_{DS}	Data Setup Time	100		ns
t_{DH}	Data Hold Time	100		ns
t_{INIT}	Write Inhibit Period After Power-up	10	30	ms

NOTE: * A write pulse of less than 20ns duration will not initiate a write cycle.

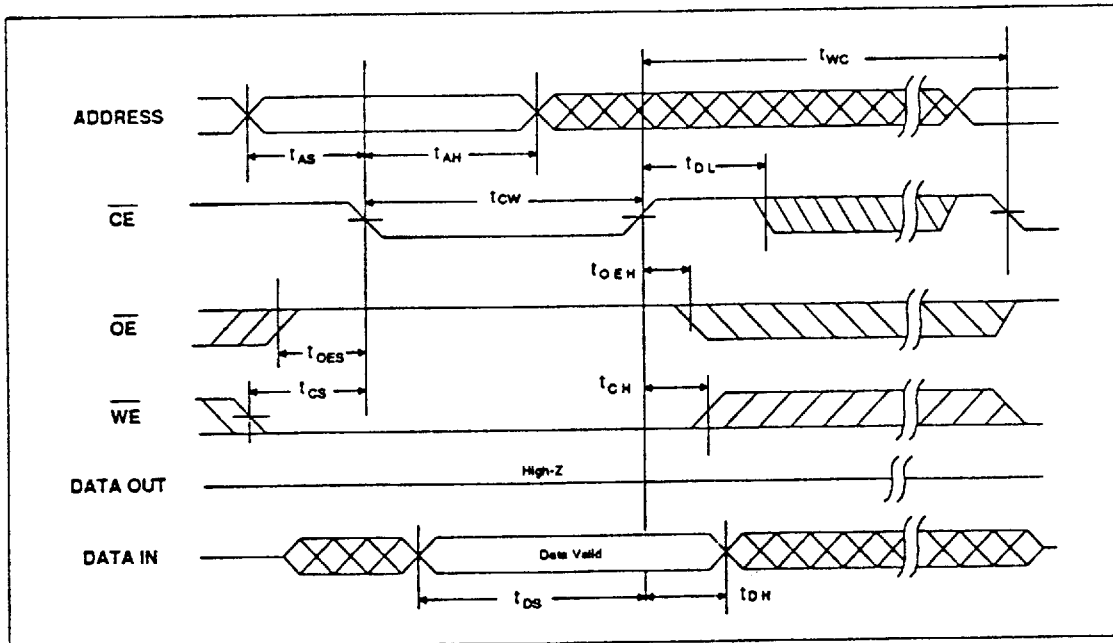
TIMING <Read Cycle>



TIMING < \overline{WE} Controlled Write Cycle>



TIMING < \overline{CE} Controlled Write Cycle>



PIN DESCRIPTIONS

ADDRESSES (A₀-A₁₀)

The Address inputs are used to select an 8-bit memory location during read and write cycles.

CHIP ENABLE (\overline{CE})

The Chip Enable input must be held LOW to enable read and write cycles. When \overline{CE} is held HIGH, the device is deselected and power consumption is reduced to the standby level.

OUTPUT ENABLE (OE)

The Output Enable input, in conjunction with \overline{CE} , determines whether the device outputs are high impedance, or output data during a read cycle.

DATA IN/DATA OUT (I/O₀-I/O₇)

Data is output to the I/O pins during a read cycle, and written into the device from the I/O pins during a write cycle.

WRITE ENABLE (WE)

The Write Enable input, in conjunction with \overline{CE} and OE, initiates a write cycle.

DEVICE OPERATION

READ

Device data is output to the data bus when both \overline{OE} and \overline{CE} are LOW. The data bus is high impedance when either \overline{CE} or \overline{OE} go HIGH. This 2-line control architecture can be used to eliminate bus contention in a system environment.

BYTE WRITE

A write cycle is initiated when both \overline{CE} and \overline{WE} are LOW and OE is HIGH. Both \overline{CE} and \overline{WE} controlled write cycles can be executed, i.e., the address is latched on the falling edge of either \overline{CE} or \overline{WE} , whichever occurs last, while data is latched on the rising edge of either \overline{CE} or \overline{WE} , whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and times itself to completion.

DATA POLLING

Data polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is in-

itiated, attempting to read the last byte written will output the complement of that data on I/O₇ (I/O₀-I/O₆ are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle all I/Os will output true data during a read cycle.

FALSE WRITE PROTECTION

(1) The CAT28C16V3 has an on-chip V_{CC} sense circuit which disables the internal write circuitry whenever V_{CC} is less than 2.0V.

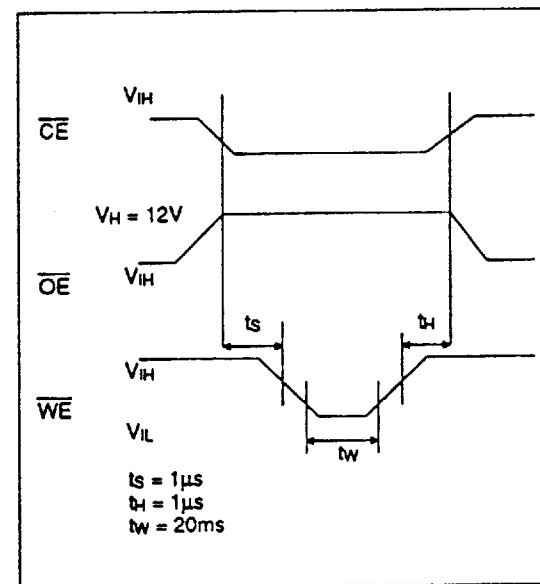
(2) During power-up, write operations are inhibited for 5ms to 20ms after V_{CC} reaches 2.0V. Read cycles are not affected during this initialization period.

(3) Write cycles are inhibited if \overline{OE} is LOW, or \overline{CE} or \overline{WE} are HIGH.

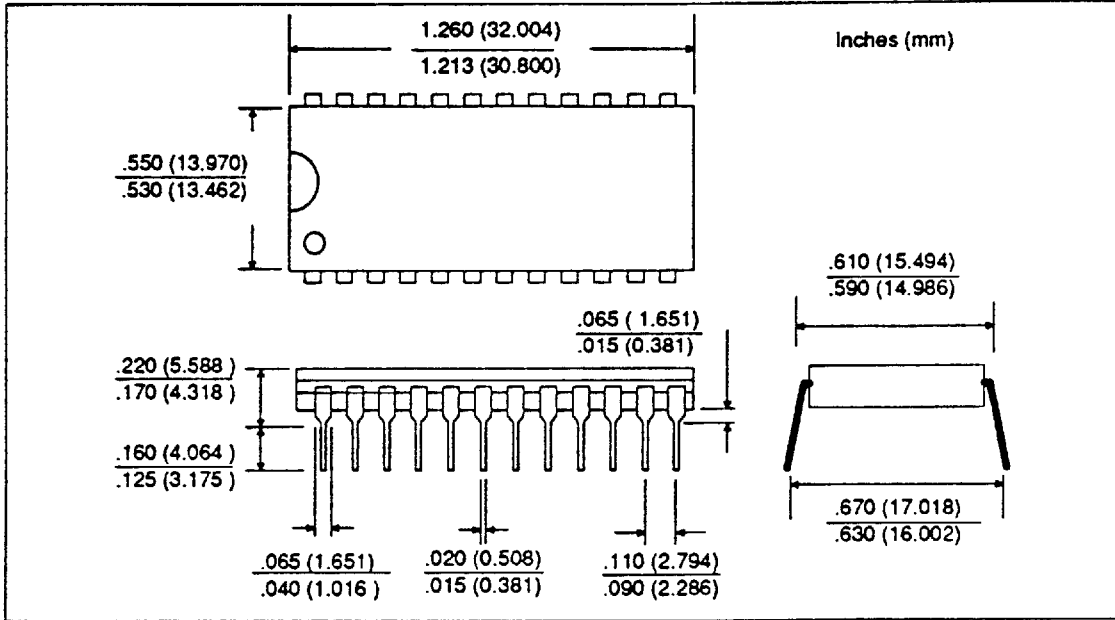
(4) A write pulse of less than 20ns duration will not initiate a write cycle.

CHIP ERASE

The entire memory can be set to 1's by setting \overline{CE} LOW, OE to 12V, and pulsing \overline{WE} LOW for 20ms.



24 PIN PLASTIC DIP



24 PIN SO

