



# PIC16FR62X

## FlexROM™-Based 8-Bit CMOS Microcontroller

### Devices included in this Data Sheet:

- PIC16FR620
- PIC16FR621
- PIC16FR622

### High Performance RISC CPU Features:

- Only 35 instructions to learn
- All single cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
  - DC - 20 MHz clock input
  - DC - 200 ns instruction cycle

Device	Program Memory	Data Memory
PIC16FR620	512	80
PIC16FR621	1K	80
PIC16FR622	2K	128

- Interrupt capability
- 16 special function hardware registers
- 8 level deep hardware stack
- Direct, indirect and relative addressing modes

### Peripheral Features:

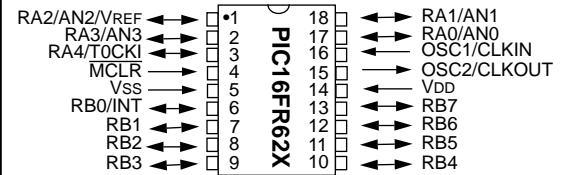
- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Analog comparator module with:
  - 2 analog comparators
  - Programmable on-chip voltage reference (VREF) module
  - Programmable input multiplexing from device inputs and internal voltage reference
  - Comparator outputs can be output signals
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler

### Special Microcontroller Features:

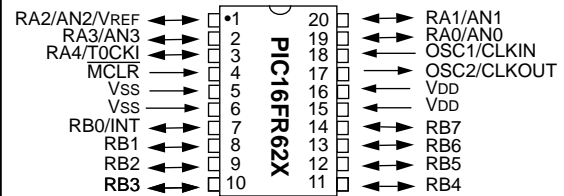
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Selectable code protection
- Power saving SLEEP mode
- Selectable oscillator options

### Pin Configurations

#### PDIP, SOIC



#### SSOP



### CMOS Technology:

- Low-power, high-speed CMOS FlexROM technology
- Fully static design
- Wide operating voltage range
  - 2.5V to 6.0V
- Commercial and industrial temperature range
- Low power consumption
  - < 2 mA @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 KHz
  - < 1 µA typical standby current @ 3V

# PIC16FR62X

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## 1.0 GENERAL DESCRIPTION

The PIC16FR62X are 18-Pin EPROM-based members of the versatile PIC16CXX family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers.

All PIC16/17 microcontrollers employ an advanced RISC architecture. The PIC16FR62X have enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with the separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16FR62X microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in its class.

The PIC16FR620 and PIC16FR621 have 80 bytes of RAM. The PIC16FR622 has 128 bytes of RAM. Each device has 13 I/O pins and an 8-bit timer/counter with an 8-bit programmable prescaler. In addition, the PIC16FR62X add two analog comparators with a programmable on-chip voltage reference module. The comparator module is ideally suited for applications requiring a low-cost analog interface, e.g. battery chargers, threshold detectors, white goods controllers, etc.

PIC16FR62X devices have special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers power saving. The user can wake-up the chip from SLEEP through several external and internal interrupts and reset.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock-up.

Table 1-1 shows the features of the PIC16FR620, PIC16FR621 and the PIC16FR622.

A simplified block diagram of the PIC16FR62X is shown in Figure 2-1.

The PIC16FR62X series fit perfectly in applications ranging from battery chargers to low-power remote sensors. The *FlexROM* technology makes customization of application programs (detection levels, pulse generation, timers, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high-performance, ease of use and I/O flexibility make the PIC16FR62X very versatile.

### 1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Code written for PIC16C5X can be easily ported to PIC16FR62X family of devices.

### 1.2 Development Support

The PIC16FR62X family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator. A "C" compiler and fuzzy logic support tools are also available.

TABLE 1-1: PIC16FR62X FAMILY OF DEVICES

	Clock			Memory				Peripherals						Features		
	Maximum Frequency of Operation (MHz)	Flash Program Memory (bytes)	Data Memory (bytes)	Timer Module(s)	Capture/Compare/PWM Module(s)	Serial Ports (SPI/I <sup>2</sup> C, USART)	Parallel Slave Port	Analog to Digital Converter (8-bit)	Comparator(s)	Internal Reference Voltage	I/O Pins	Voltage Range (Volts)	Brown-out Detect	Packages		
PIC16FR620	20	512	80	—	—	—	—	2	Yes	4	13	2.5-6.0	Yes	18-pin DIP, SOIC, 20-pin SSOP		
PIC16FR621	20	1K	80	—	—	—	—	2	Yes	4	13	2.5-6.0	Yes	18-pin DIP, SOIC, 20-pin SSOP		
PIC16FR622	20	2K	128	—	—	—	—	2	Yes	4	13	2.5-6.0	Yes	18-pin DIP, SOIC, 20-pin SSOP		

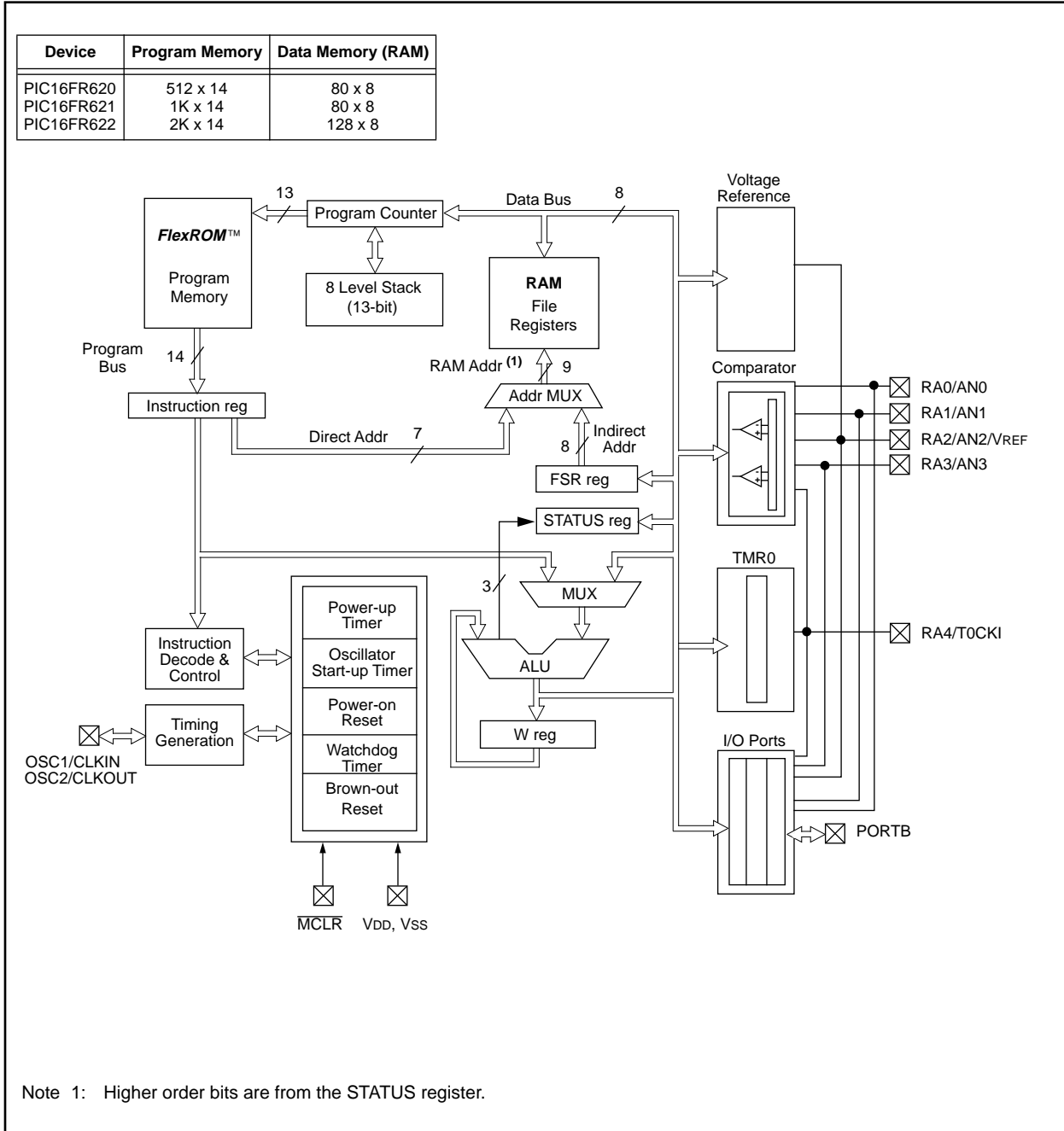
**Note:** All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

# PIC16FR62X

## 2.0 ARCHITECTURAL OVERVIEW

This section provides information on the architecture of the PIC16FR62X. For information on operation of the peripherals, electrical specifications, etc., please refer to the PIC16C62X data sheet (DS30235C).

**FIGURE 2-1: PIC16FR62X BLOCK DIAGRAM**



**TABLE 2-1: PIC16FR62X PINOUT DESCRIPTION**

Name	DIP SOIC Pin #	SSOP Pin #	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	18	I	ST/CMOS	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR	4	4	I/P	ST	Master clear (reset) input. This pin is an active low reset to the device.
RA0/AN0	17	19	I/O	ST	PORTA is a bi-directional I/O port. Analog comparator input Analog comparator input Analog comparator input or VREF output Analog comparator input /output Can be selected to be the clock input to the Timer0 timer/counter or a comparator output. Output is open drain type.
RA1/AN1	18	20	I/O	ST	
RA2/AN2/VREF	1	1	I/O	ST	
RA3/AN3	2	2	I/O	ST	
RA4/T0CKI	3	3	I/O	ST	
RB0/INT	6	7	I/O	TTL/ST <sup>(1)</sup>	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. RB0/INT can also be selected as an external interrupt pin.  Interrupt on change pin. Interrupt on change pin. Interrupt on change pin. Interrupt on change pin.
RB1	7	8	I/O	TTL	
RB2	8	9	I/O	TTL	
RB3	9	10	I/O	TTL	
RB4	10	11	I/O	TTL	
RB5	11	12	I/O	TTL	
RB6	12	13	I/O	TTL/ST	
RB7	13	14	I/O	TTL/ST	
Vss	5	5,6	P	—	Ground reference for logic and I/O pins.
VDD	14	15,16	P	—	Positive supply for logic and I/O pins.

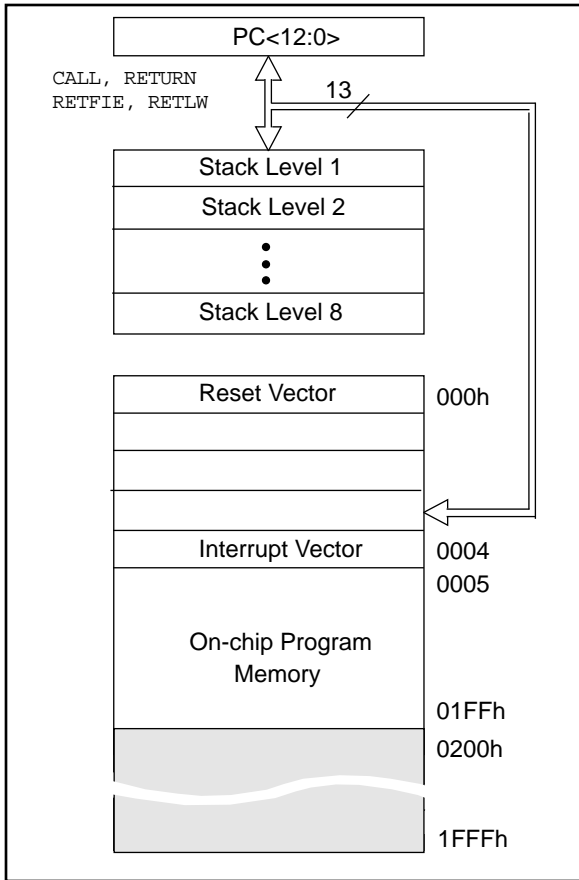
Legend:            O = output                            I/O = input/output            P = power  
                      — = Not used                        I = Input                        ST = Schmitt Trigger input  
                      TTL = TTL input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

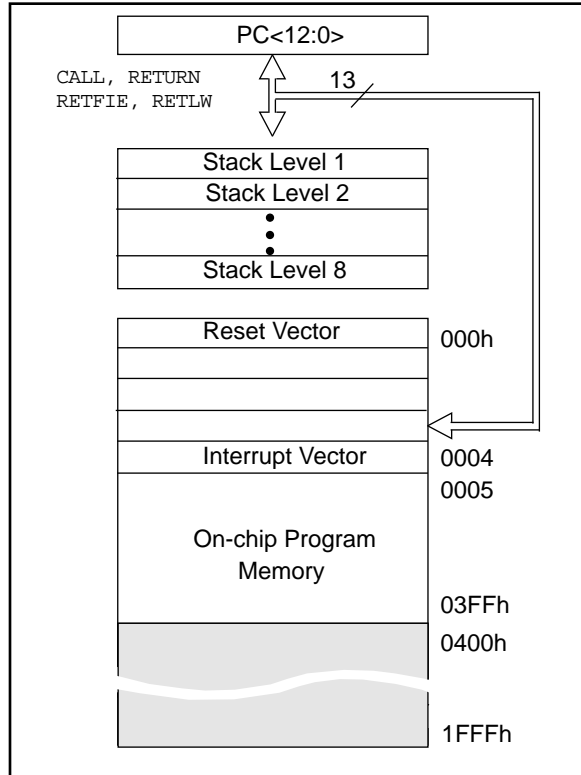
# PIC16FR62X

## 3.0 MEMORY ORGANIZATION

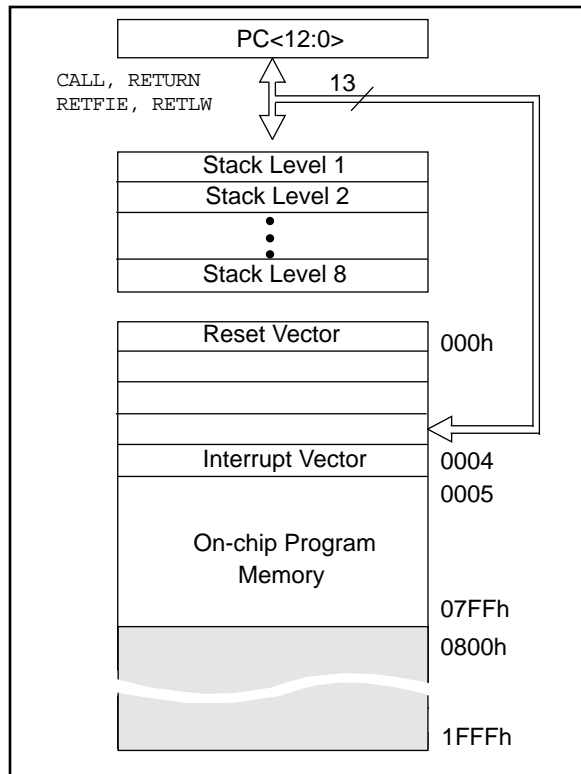
**FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16FR620**



**FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC16FR621**



**FIGURE 3-3: PROGRAM MEMORY MAP AND STACK FOR THE PIC16FR622**



**FIGURE 3-4: DATA MEMORY MAP FOR THE PIC16FR620/621**

File Address			File Address	
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h	
01h	TMR0	OPTION	81h	
02h	PCL	PCL	82h	
03h	STATUS	STATUS	83h	
04h	FSR	FSR	84h	
05h	PORTA	TRISA	85h	
06h	PORTB	TRISB	86h	
07h			87h	
08h			88h	
09h			89h	
0Ah	PCLATH	PCLATH	8Ah	
0Bh	INTCON	INTCON	8Bh	
0Ch	PIR1	PIE1	8Ch	
0Dh			8Dh	
0Eh		PCON	8Eh	
0Fh			8Fh	
10h			90h	
11h			91h	
12h			92h	
13h			93h	
14h			94h	
15h			95h	
16h			96h	
17h			97h	
18h			98h	
19h			99h	
1Ah			9Ah	
1Bh			9Bh	
1Ch			9Ch	
1Dh			9Dh	
1Eh			9Eh	
1Fh	CMCON	VRCON	9Fh	
20h	General Purpose Register		A0h	
6Fh				BFh
70h				C0h
7Fh			FFh	

Bank 0                      Bank 1

Unimplemented data memory locations, read as '0'.  
 Note 1: Not a physical register.

**FIGURE 3-5: DATA MEMORY MAP FOR THE PIC16FR622**

File Address			File Address	
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h	
01h	TMR0	OPTION	81h	
02h	PCL	PCL	82h	
03h	STATUS	STATUS	83h	
04h	FSR	FSR	84h	
05h	PORTA	TRISA	85h	
06h	PORTB	TRISB	86h	
07h			87h	
08h			88h	
09h			89h	
0Ah	PCLATH	PCLATH	8Ah	
0Bh	INTCON	INTCON	8Bh	
0Ch	PIR1	PIE1	8Ch	
0Dh			8Dh	
0Eh		PCON	8Eh	
0Fh			8Fh	
10h			90h	
11h			91h	
12h			92h	
13h			93h	
14h			94h	
15h			95h	
16h			96h	
17h			97h	
18h			98h	
19h			99h	
1Ah			9Ah	
1Bh			9Bh	
1Ch			9Ch	
1Dh			9Dh	
1Eh			9Eh	
1Fh	CMCON	VRCON	9Fh	
20h	General Purpose Register	General Purpose Register	A0h	
6Fh				BFh
70h				C0h
7Fh			FFh	

Bank 0                      Bank 1

Unimplemented data memory locations, read as '0'.  
 Note 1: Not a physical register.

# PIC16FR62X

**TABLE 3-1: SPECIAL REGISTERS FOR THE PIC16FR62X**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR Reset	Value on all other resets <sup>(1)</sup>
<b>Bank 0</b>											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
01h	TMR0	Timer0 Module's Register								xxxx xxxx	uuuu uuuu
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h	STATUS	IRP <sup>(2)</sup>	RP1 <sup>(2)</sup>	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	$\overline{RA4}$	$\overline{RA3}$	$\overline{RA2}$	$\overline{RA1}$	RA0	---x xxxx	---u uuuu
06h	PORTB	RB7	RB6	RB5	$\overline{RB4}$	$\overline{RB3}$	$\overline{RB2}$	$\overline{RB1}$	RB0	xxxx xxxx	uuuu uuuu
07h	Unimplemented									—	—
08h	Unimplemented									—	—
09h	Unimplemented									—	—
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter				---0 0000	---0 0000	
0Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000x
0Ch	PIR1	—	CMIF	—	—	—	—	—	—	-0-- ----	-0-- ----
0Dh-1Eh	Unimplemented									—	—
1Fh	CMCON	C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0	00-- 0000	00-- 0000
<b>Bank 1</b>											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
81h	OPTION	$\overline{RBP}$	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
87h	Unimplemented									—	—
88h	Unimplemented									—	—
89h	Unimplemented									—	—
8Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter				---0 0000	---0 0000	
8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000x
8Ch	PIE1	—	CMIE	—	—	—	—	—	—	-0-- ----	-0-- ----
8Dh	Unimplemented									—	—
8Eh	PCON	—	—	—	—	—	—	POR	BOR	---- -0x	---- -uq
8Fh-9Eh	Unimplemented									—	—
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

**Note 1:** Other (non power-up) resets include  $\overline{MCLR}$  reset, Brown-out Rreset and Watchdog Timer Reset during normal operation.

**Note 2:** IRP & RPI bits are reserved, always maintain these bits clear.

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In the United States, to find CompuServe's phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600-14400 baud connection. After the system responds with *Host Name:*

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# PIC16FR62X

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## PIC16FR62X Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NO.	-XX	X	/XX	XXX	
					<b>Pattern:</b> 3-Digit Pattern Code for <i>FlexROM</i>
					<b>Package:</b> P = PDIP SO = SOIC (Gull Wing, 300 mil body) SS = SSOP (209 mil)
					<b>Temperature Range:</b> - = 0°C to +70°C I = -40°C to +85°C
					<b>Frequency Range:</b> 04 = 200kHz (LP osc) 04 = 4 MHz (XT and RC osc) 20 = 20 MHz (HS osc)
					<b>Device:</b> PIC16FR62X: VDD range 4.0V to 6.0V PIC16FR62XT: VDD range 4.0V to 6.0V (Tape and Reel) PIC16LFR62X: VDD range 3.0V to 6.0V PIC16LFR62XT: VDD range 3.0V to 6.0V (Tape and Reel)

**Examples:**

a) PIC16FR62X - 04/P 301 = Commercial temp., PDIP package, 4 MHz, normal VDD limits, pattern #301.

b) PIC16LFR62X- 04I/SO 512 = Industrial temp., SOIC package, 200kHz, extended VDD limits, pattern #512.

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Tel: 81 45 471 6166 Fax: 81 45 471 6122

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